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Report No. FHWA-RD-77-122

# VEHICLE DETECTION PHASE III: PASSIVE BUS DETECTOR/INTERSECTION PRIORITY SYSTEM DEVELOPMENT

## Option II: Manufacturing Drawings and Prototype Development



October 1977  
Final Report

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Prepared for  
FEDERAL HIGHWAY ADMINISTRATION  
Offices of Research & Development  
Washington, D. C. 20590

## FOREWORD

This report is the result of a contract with Honeywell, Inc. to develop a Passive Bus Detector and Intersection Priority system. The system functions as a fully independent traffic controller with completely passive bus detection capability (i.e. with no special equipment required on the bus) using inductive loop detectors (ILD) placed in the roadway.

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Director, Office of Research

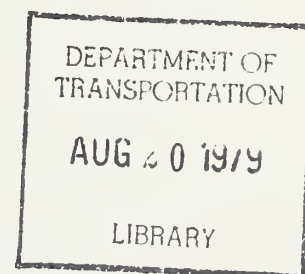
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16. Abstract  A production prototype 16-channel Passive Bus Detector (PBD) was developed, based on the engineering model Passive Bus Detector/Intersection Priority System. The PBD is functionally the same as the engineering model except that the traffic controller function was not carried along into the production prototype mode. The PBD was repackaged to facilitate production and evaluated in an intersection with a typical traffic controller. Operation in the intersection for a 2-month period was successful.					
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## SECTION 1

### INTRODUCTION

This final report covers Option II of Phase III of the Vehicle Detection Project. The Vehicle Detection Project, Contract No. DOT-FH-11-8149, is a contract between Honeywell Inc. and the Federal Highway Administration. Phase III is entitled "Passive Bus Detector/Intersection Priority System." Option II is entitled "Manufacturing Drawings and Prototype Development." The contract period for Option II was 30 November 1976 to 31 October 1977. D. O. Wick was the Project Manager.

Other personnel assigned to Option II were:

- R. A. Lubke - Principal Investigator
- D. D. Sawyer - Senior Systems Engineer
- D. G. Putnam - Development Engineer
- W. D. Everhart - Principal Development Engineer
- J. C. Walter - Evaluation Engineer

## SECTION 2

### SUMMARY

This report presents the results of the effort to develop a production prototype model of the Passive Bus Detector (PBD). This model is the outgrowth of the Passive Bus Detector/Intersection Priority System which was developed in the earlier part of this contract. The original PBD concept included a traffic controller as an integral part of the device. In the production prototype model reported herein, the system concept was reconfigured to remove the controller, thus making bus preemption a more flexible system in terms of hardware systems configuration. The 16-channel capacity of the PBD, however, was retained.

A driving force during Option II was to reduce the production costs as much as possible. As a result, several interesting equipment packaging concepts were formulated. These are discussed later in this report.

The basic building block modules were changed very little from the previous model. The National Semiconductor IMP-16C microcomputer was retained for use in the classifier unit. Also, the concept of four-pack inductive-loop electronics operating with a 16-channel classifier was retained.

### SECTION 3

#### OBJECTIVE

The objective of Option II was to reduce the engineering model Passive Bus Detector/Intersection Priority System, which was developed in the earlier portion of this contact, to a production prototype model. This means that: 1) the system had to be documented to a sufficient level such that additional units could be manufactured from the drawings and, 2) mechanical and electronic subassemblies be refined for production environment.

In addition, the production prototype model was evaluated in a typical traffic intersection with a typical traffic controller. This evaluation was to verify that the performance of the production prototype model was equal to, or better than, the engineering model.

## SECTION 4

### SYSTEM DESCRIPTION

The Passive Bus Detector is a stand-alone, microprocessor-based system for passively detecting the presence of widely used 40- to 60-ft. mass busses on a roadway. Although the PBD was developed to operate with busses manufactured by GMC, AMC and Flexible, it can be adapted to other bus types and manufacturers should the need arise. The PBD uses the well-known inductive-loop transducer. No bus driver cooperation is required other than driving the bus over the detection zone of the loop(s).

The PBD system consists of two components: 1) a 16-channel Bus Classifier Unit (BCU) (Figure 1), and 2) special inductive-loop electronics in the form of the Inductive-Loop Detector Unit (ILDU) shown in Figure 2.

#### 4.1 BUS CLASSIFIER UNIT

BCU contains the PBD system intelligence. Two microprocessors operating in tandem make up the major building blocks of the BCU. They receive analog detector information from a maximum of 16 inductive-loop electronics. The BCU determines vehicle presence and determines whether or not the vehicle is a bus. This information is returned to the respective loop electronics for further action.

The BCU has two controls available to the operator: a System Test Switch and a System Clear Switch. The System Test switch initiates a system self-test whose response is monitored by the operator. The System Clear switch simulates the power restart function which initializes the PBD system. These switches are discussed further in Section 5, Technical Discussion.



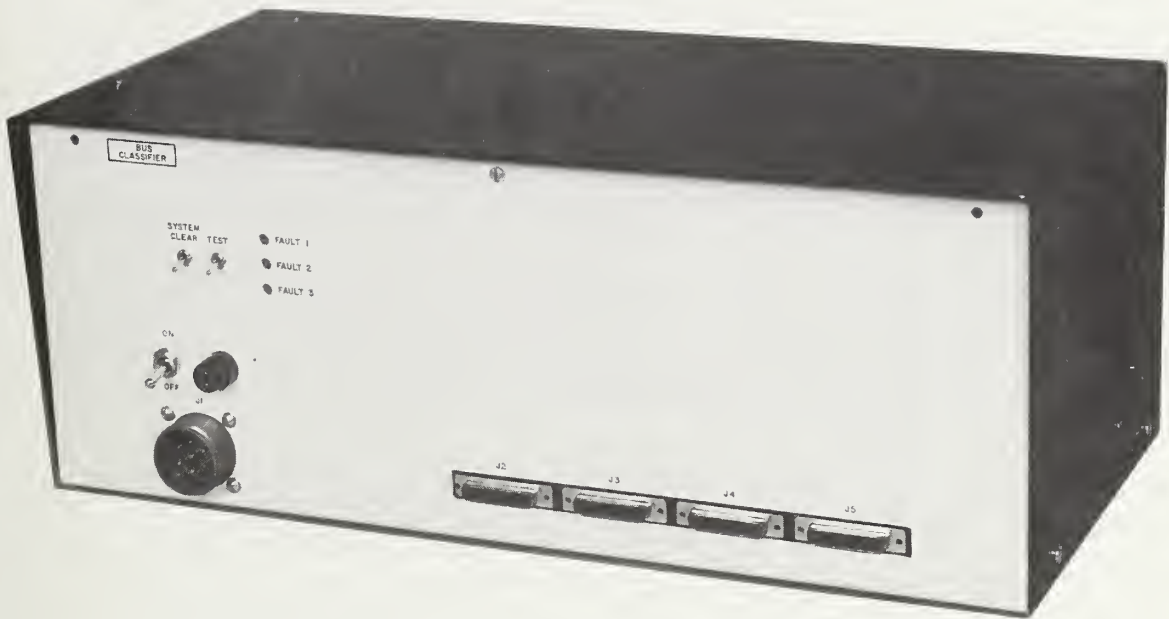


Figure 1. Bus Classifier Unit



Figure 2. Inductive-Loop Detector Unit

Three BCU fault indicators appear on the front panel for the operator. The fault signals are also in the power connector, J1, for remote sensing. J1 also contains a remote reset input which performs a system clear function. These functions are also discussed in Section 5, Technical Discussion.

## 4.2 INDUCTIVE LOOP DETECTOR

The Inductive Loop Detector (ILD) is a high-quality phase detector which drives the inductive loop and extracts changes in loop inductance due to vehicle presence. The ILDU consists of a power supply section plus space for four ILDs. The four-pack packaging concept was chosen as a compromise between three considerations:

- Most applications of bus preemption will require more than one detectorized approach, but less than 16.
- A 16-pack ILDU would be relatively expensive for minimum configuration systems.
- A four-pack ILDU imposes medium design requirements on the power supply section.

As a result of the selection of this packaging concept (each ILD was designed to be pluggable), the traffic engineer is able to select the exact number of detectors for his system, or, if he desires, may upgrade his system at minimum expense.

Several indicators and controls are available to the operator on the front of the ILDU. The three light-emitting diodes (LED) indicators on the front of each ILD are: Bus Call, Vehicle Call, and Tune Limit. The Tune Limit indicator is used in tuning the loop and lead-in. A meter

on the power supply section and an associated selector switch complete the tuning indicators. Three thumbwheel switches on each ILD constitute the front-panel tuning controls. (See Appendix A for tuning compensation derivations.)

A screwdriver adjustment on the front of each ILD allows the operator to change sensitivity (gain). The remaining control allows the operator to change the vehicle call relay closure duration.

The PBD system interfaces with the traffic controller via the ILDU power supply section. One bus call and one vehicle call relay are available for each ILD.

Additional detail is covered in Section 5, Technical Discussion, concerning theory of operation, detector tuning, and setup operations.

## SECTION 5

### TECHNICAL DISCUSSION

#### 5.1 INTRODUCTION

The PBD system consisting of a BCU and one to four ILDU's has a simple system structure. The BCU acts as a supporting subsystem to the ILDU's. However, to the traffic engineer and to control systems in the intersection cabinet, the PBD system merely appears as smart ILDs. This is because all PBD interfacing with other systems, such as the traffic controller, is done through the ILDU's. Figure 3 shows this relationship more clearly. The loops from the roadway go to the ILDU and the bus/no-bus decision comes via the relays in the ILDU.

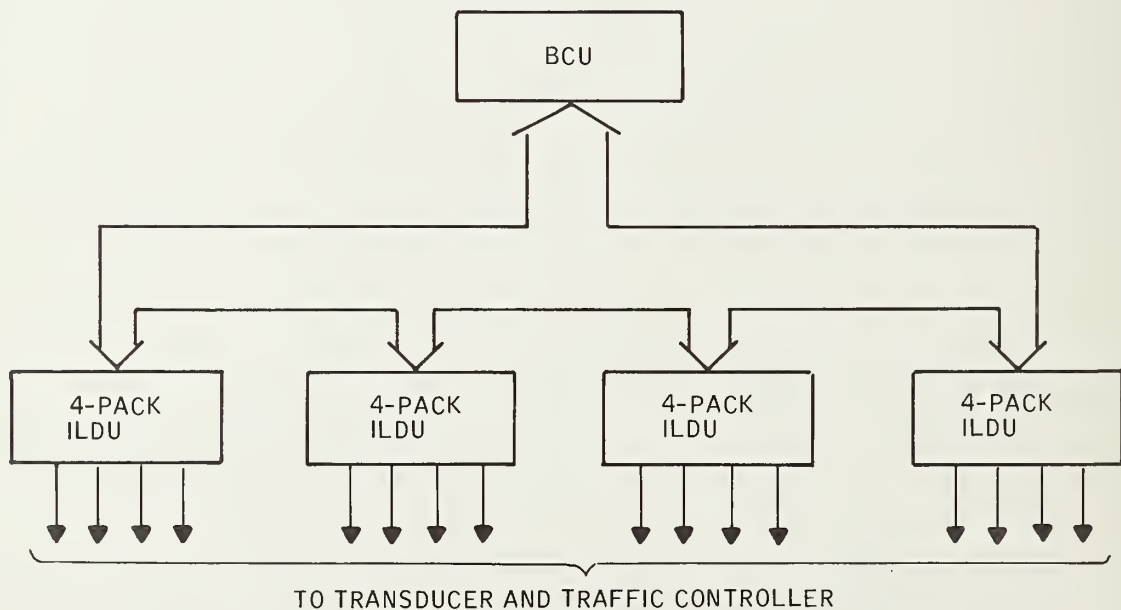


Figure 3. PBD Interconnect Diagram



The discussion of the theory of operation of the PBD system will be broken into these two subsystems. Each subsystem will be treated as an entity but can be related back to Figure 3. Figure 4 defines this relationship even further.

## 5.2 ILDU

The ILDU consists of a power supply and chassis with one to four ILDs; the power supply is shared.

### 5.2.1 Power Supply

Power supply operation is discussed with reference to its schematic (Drwg. No. 10059902, see Appendix B).

The power supply delivers two voltages for the ILDU. Unregulated 25 VDC is supplied for use by the vehicle and bus call relays (R11, et al.) and all LEDs. Transformer T1 and power rectifier diodes, CR10 and CR11, supply a nominal 25 VDC at 115 VAC input. Monolithic voltage regulator, U1, in conjunction with pass transistor, Q<sub>2</sub>, supplies regulated 12 VDC  $\pm$  0.5% for use by the ILD electronics.

Q1, CR1, and R1 constitute the typical relay driver circuit. U2 is a buffer amplifier for meter M1. Switch S1 selects the desired ILD output to be monitored.

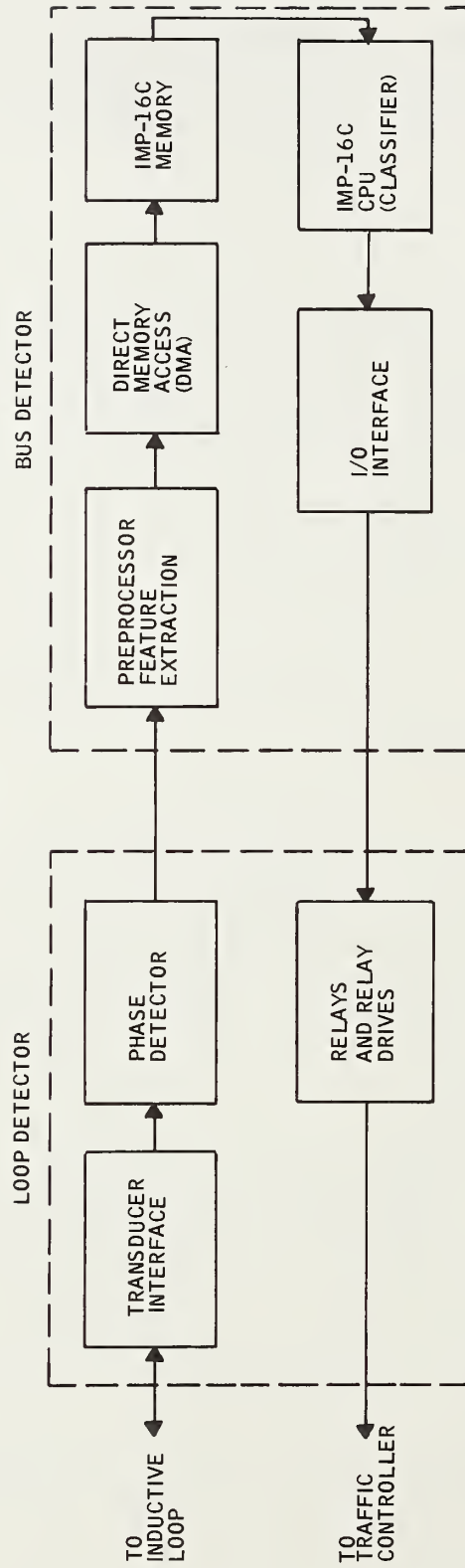


Figure 4. PBD Data Flow

### 5.2.2 Inductive-Loop Detector

ILD operation is discussed with reference to its schematic (Drwg. No. 10059903, see Appendix B). Figure 5 is a block diagram of the ILD loop transducer circuits.

A crystal oscillator, U3, operating at  $2f_0$  is divided by two by flip-flop U2. U2 supplies both a reference signal to phase detector U4 and the loop driver U3. Thumbwheel switches S1, S2, and S3 select the appropriate tuning capacitors, C1 through C12, for loop resonance. Jumper J1 provides additional capacitance for short loop lead-ins. The circuit consisting of R23, R24, CR5, CR4, and D51 is to suppress high-voltage transients (such as lightning) which might appear at the loop inputs. Transformer T1 takes the common mode signal off the loop to the zero-crossing detector, U6. The loop signal is further shaped by U4 and sent to the phase detector, U4, and flip-flop U2. The output of the phase detector is integrated by network R13, R14, and C5 and amplified by U5. Jumper J2 selects a high/low sensitivity range for the ILD.

Flip-flop U4 is used to determine when the phase detector output is on the wrong side of null.

Monostable multivibrators U1, and in conjunction with switch S4, determine the length of time the vehicle call relay is energized (short, medium, long).

### 5.3 BUS CLASSIFIER UNIT

The BCU is organized around the National Semiconductor IMP-16C micro-computer. A block diagram of the operational structure (Figure 6) shows the bus-oriented nature of the BCU. The BCU is an interrupt-driven system. Figure 7 shows the order of card locations in the chassis.

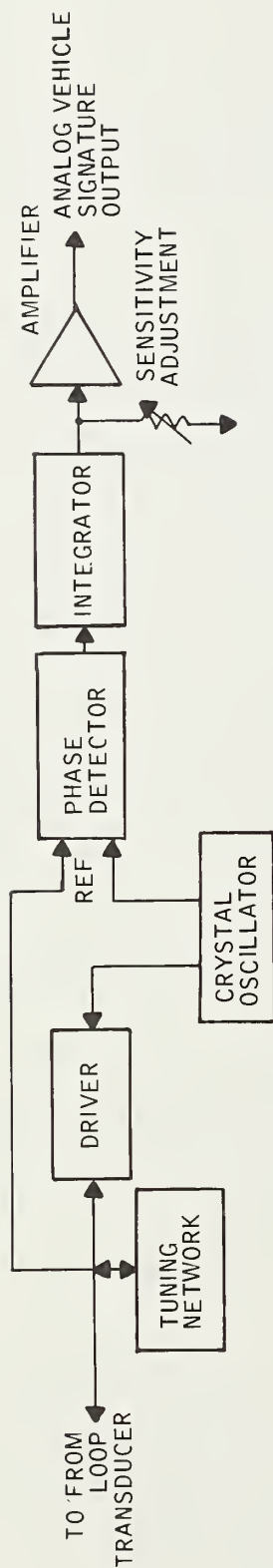


Figure 5. ILD Block Diagram

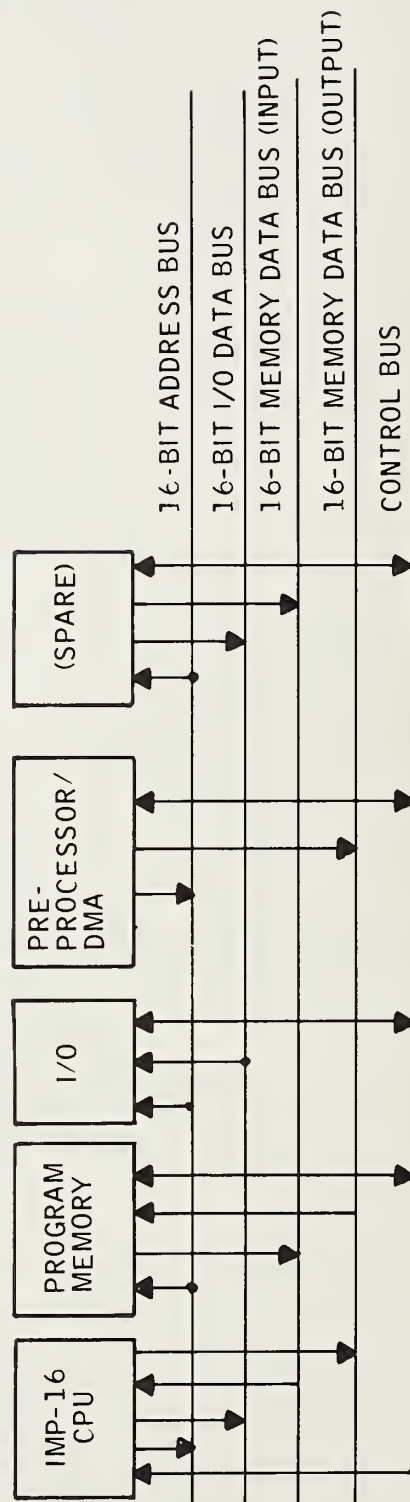


Figure 6. IMP-16C Bus Structure



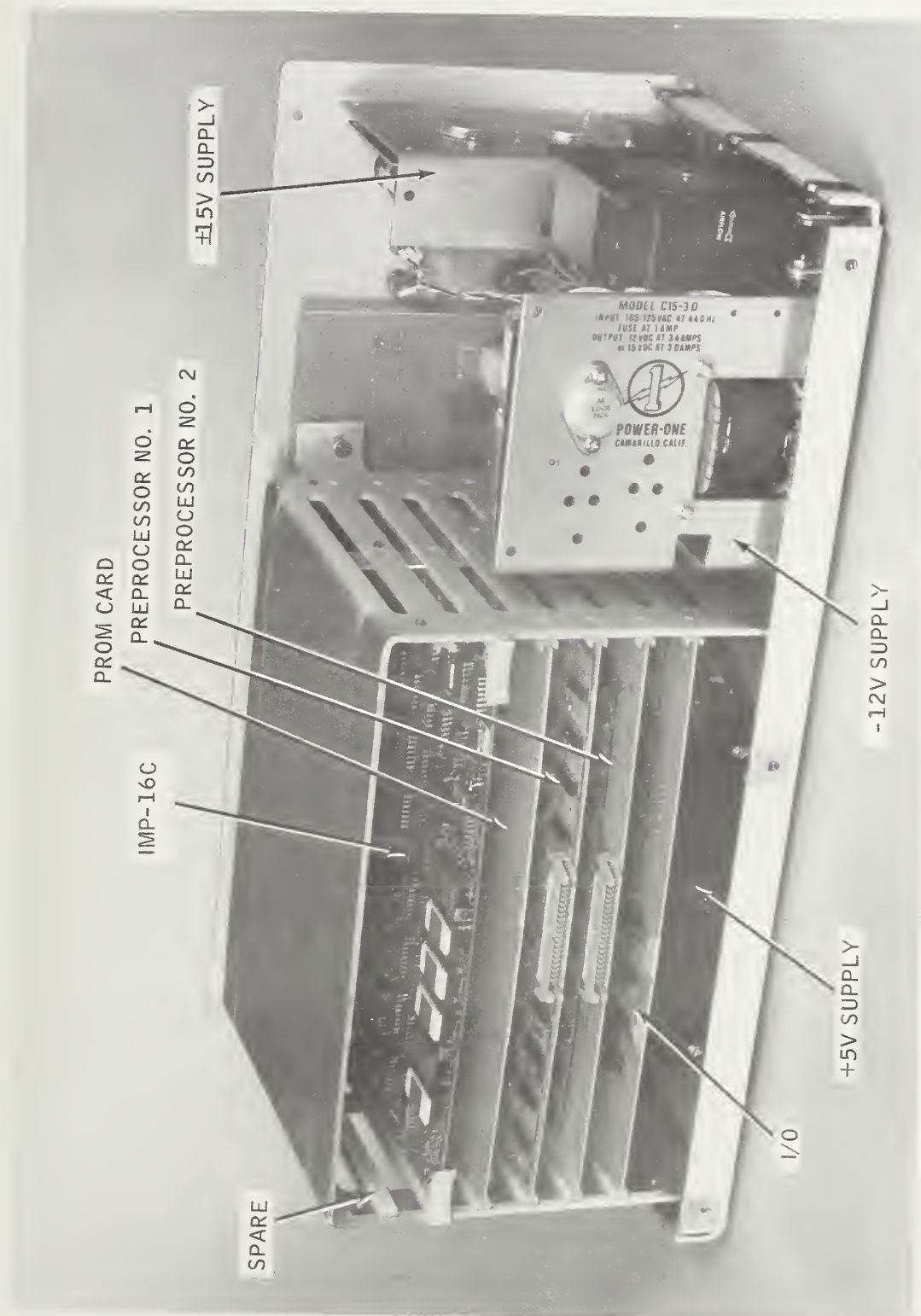


Figure 7. BCUCard Locations

### 5.3.1 Input/Output (I/O) Module

I/O module operation is discussed with reference to the I/O schematic (Drwg. No. 10059899, see Appendix B). Three functions are performed on this card: 1) system autorestart, 2) real-time clock and 3) ILD relay driver interface.

The autorestart circuit monitors the +5V supply for low voltage via comparator 4C and R23. When low voltage is detected, 4C trips flip-flop 6C. Recovery time is governed by CR2, R13, and C14. The output of the autorestart circuit is "OR"ed with the system clear switch, S1, and goes to other BCU cards. Autorestart can also be initiated by the central processor unit (CPU) via flag 13 and monostable multivibrator 6D. CPU-generated autorestart can be inhibited by switch S3.

Flip-flop 8D (left half) monitors the occurrence of a CPU-initiated autorestart and drives fault 2 indicator.

Flip-flop 8D (right half) monitors the occurrence of a CPU-diagnosed random-access memory (RAM) error via flag 11 and drives fault 1 indicator.

A 0.2 second-period real-time clock for the BCU is made of gated astable multivibrator 7A and flip-flop 9A. 9A drives the CPU general interrupt line until it is cleared by the CPU via 9B or stopped by the CPU via 10B.

Hex flip-flops 2B through 5B are the latches for bus/vehicle output for each ILD; 1A through 5A are open collector buffers.

Circuits 8B, 8C, and 9C are address decoders which decipher what function is to be performed on the I/O card. Debounce flip-flop 8B with switch S1 is a CPU jump condition input for diagnostic purposes. Debounce flip-flop 10A and switch S2 form the System Test circuit located on the BCU front panel.

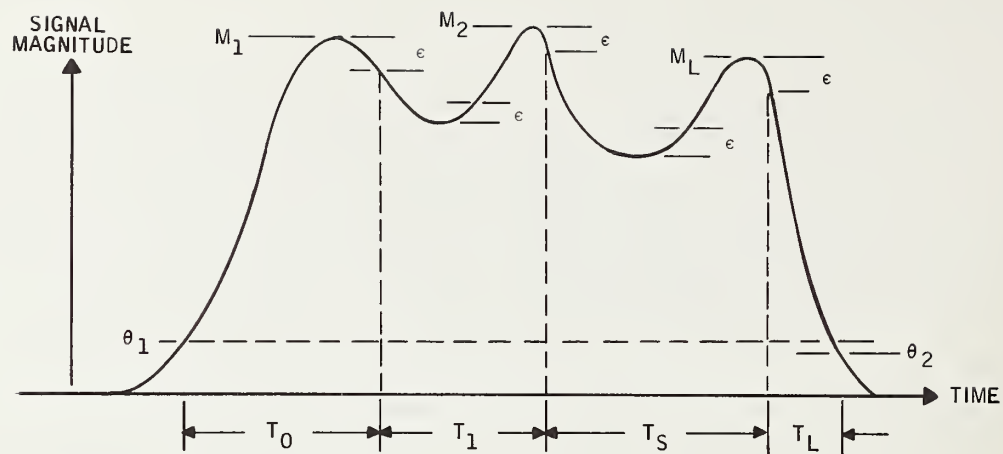
### 5.3.2 Preprocessor Module

The primary purpose of the preprocessor is to extract the important features from each loop detector signal, up to a maximum of 16 ILDs, and store these features in the IMP-16C memory. Figure 8 is a sketch of an idealized bus signature showing the primary signature features extracted. These features are the values of the signature peaks and their associated time intervals. The secondary function of the preprocessor is to determine vehicle presence. Presence information is sent to the IMP-16C memory for processing.

The preprocessor consists of two printed-circuit cards. These cards contain the analog interface with the loop detectors (ILDs) and the direct-memory access (DMA) interface with the IMP-16C RAM, among other functions. Figure 9 is a block diagram of the preprocessor showing the gross partitioning of the functions on each card.

Card 1 is represented by schematic diagram 10059904 (see Appendix B). On sheet 1, 3C and 4C compromise the program counter which feeds a latch, 3D and 4D. The preprocessor program is contained in programmable read-only memories (PROMs) 2B, 3B, and 4B. Since the preprocessor is actually a microprocessor, these PROMs may be removed and replaced with a set of diagnostic PROMs. A diagnostic can speed the production checkout process. 2A, 3A, and 4A decode the program instructions and control the individual registers, memory, etc., in the remainder of the preprocessor. 1C and 1B, with associated circuitry, generate the preprocessor clocks which control the timing of the preprocessor. 5E, 6E, and associated circuitry generate and control the 250- $\mu$ sec interrupt for polling of the detectors.

Sheet 2 shows the arithmetic logic units (ALUs), 7A, 8A, and 9A, and associated support registers, 6A, 10A, 5A, 11A, 7B, 8B, and 9B. 6B and 10B is a general-purpose register which is used for temporary data storage.



#### PRIMARY FEATURES

- $T_0$  = TIME FROM TURN-ON TO FIRST PEAK
- $T_1$  = TIME FROM FIRST PEAK TO SECOND PEAK
- $T_S$  = TIME FROM SECOND PEAK TO LAST PEAK
- $T_L$  = TIME FROM LAST PEAK TO TURN-OFF
- $M_1$  = MAGNITUDE OF FIRST PEAK
- $M_2$  = MAGNITUDE OF SECOND PEAK
- $M_L$  = MAGNITUDE OF LAST PEAK

Figure 8. Bus Signature Primary Features

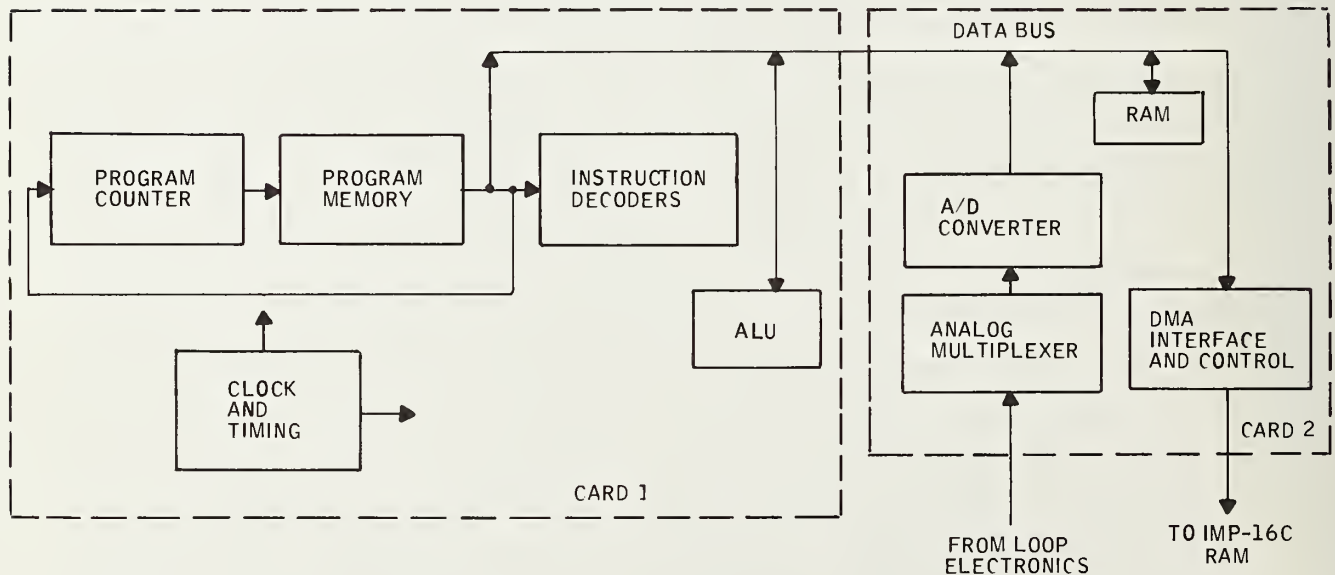


Figure 9. Preprocessor Block Diagram



6C and 9C are additional instruction decoders for preprocessor control. 10F is a flag register and feeds 11F, the jump multiplexer. 10C, 5C, 11B, 5B, and 11C are tristate data buffers. The T-switch sets the threshold voltage (above background) at which vehicle presence is detected ( $\theta_1$  of Figure 8). The E-switch selects the sensitivity of the peak detector routine ( $\epsilon$  of Figure 8).

Card 2 is represented by schematic diagram 10059901 (see Appendix B). On sheet 1, the DMA interface control is shown. 11D latches a DMA request under program control. When the IMP-16C is not using memory, 9B enables shift register 10D, which generates the timing signals for the DMA cycle. 9B (right half) controls the data and address bus drivers located on sheet 2.

Sheet 2 shows the 16-channel analog multiplexer, 4A, and A/D converter, 2C. 3B and 4C are tristate data buffers. 4B and 7C comprise the RAM address register for RAM 5D, 6D, and 7D. The DMA address register is 5B and 8B with bus drivers 7A, 8A, and 10C. The DMA data register is 2B and 6B with bus drivers 6A, 2A, and 5A.

The preprocessor program listing is found in Appendix C.

### 5.3.3 PROM Memory Module

PROM memory operation is discussed with reference to its schematic (Drwg. 1005990, see Appendix B). This card contains all PROM memory for the IMP-16 CPU. Memory chips 1C through 10C are erasable PROMs. 4A and 5A are address buffers. 6C and 8C are address decoders which select the memory chip pair in which the desired data are located.

1A, 2A, and 3A are tristatable memory output data buffers.

Circuits 7A, 8A, and 9A are buffers for the debug card, general interrupt circuit, and the DMA.

#### 5.3.4 Central Processor Unit Module

The theory of operation of the IMP-16C is covered in detail in Volume II, "IMP-16C Application Manual." This subsection will therefore treat only the general aspects of the IMP-16C.

Figure 10 is a block diagram of the CPU card, showing the major functions on it. These major functions are:

- CPU
- Clock generators
- Input multiplexer
- Data buffer
- Control flags
- Conditional jump multiplexer
- On-card memory
- Address latches

The CPU is configured around the National Semiconductor GPC/P (general-purpose controller/processor) metal-oxide semiconductor/large-scale integrated (MOS/LSI) devices, as shown in the block diagram. The MOS/LSI devices consist of one CROM (control read-only memory) and four RALUs (register and arithmetic logic units). Each RALU handles four bits, and a 16-bit unit is formed by connecting four RALUs in parallel. A 4-bit-wide control bus is used by the CROM to communicate most of the control information to the RALUs. The CPU includes provision for adding a second CROM for an optional extended instruction set which is used in this system.

The clock generator provides the MOS clock drivers and CPU timing signals. The system clock is distributed outside of the IMP-16C for synchronization of peripheral units with the IMP-16C.



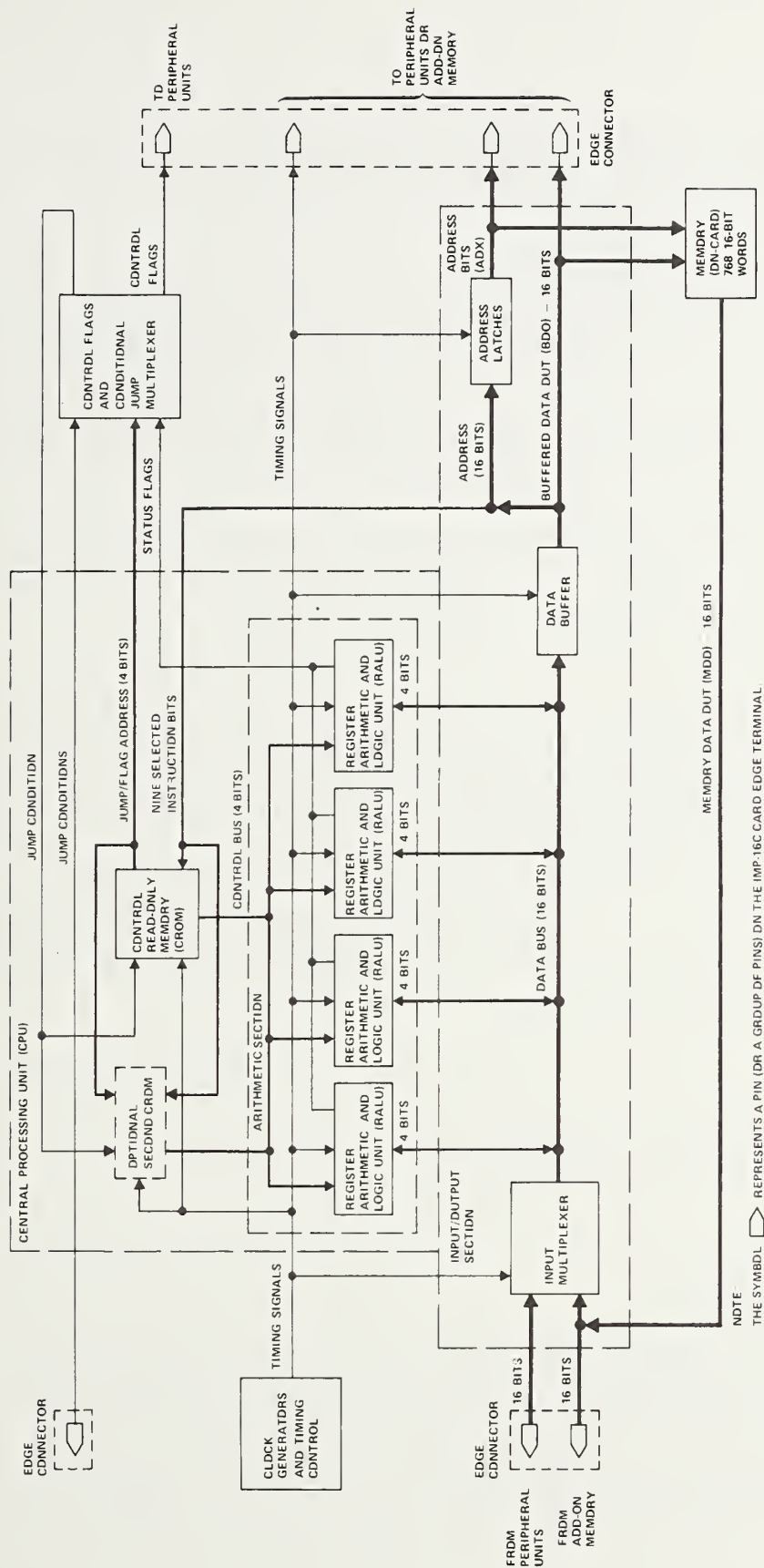


Figure 10. IMP-16C Simplified Block Diagram

External to the MOS/LSI circuits but still within the IMP-16C are control flags for both the IMP-16C and external interfacing circuits.

These control flags are in addition to the status flags that are internal to the RALUs. The status flags are discussed in the description of the CPU. The control flags are discussed under the control flag instructions. Conditional branches are selected by the conditional jump multiplexer. These branch conditions are discussed in under the Branch-On-Condition (BOC) instruction.

Data from the user's peripheral devices and add-on memory are received by the input multiplexer. Data from the on-card memory are also processed through the input multiplexer enroute to the CPU.

Output data are made available from the 16-bit data buffer via the card-edge connector to the user's peripheral devices and add-on memory. A 16-bit address bus is also brought out to the card-edge connector for addressing both add-on memory and peripheral devices.

The memory on the IMP-16C card consists of 1024 words of read/write memory and sockets for 1024 words of PROM or ROM. A maximum of 65, 536 words may be addressed.

## 5.4 PROGRAM DOCUMENTATION

### 5.4.1 Identification

This section describes the computer program for the Passive Bus Detector Production Prototype unit. This software is operational in the micro-computer unit (MCU) of the Bus Classifier Unit (BCU) and is written in assembler language for the IMP-16 MCU.

The software is written in accordance with the FHWA software documentation standard.

#### 5.4.2 Functional Summary

This program detects vehicles and transit busses, while operating real time, and sends signals to the intersection control system to indicate the presence of a vehicle, and whether or not that vehicle is a transit bus for each of up to 16 loops.

#### 5.4.3 Memory Map

The allocation of the MCU memory, the memory address ranges, and memory type are shown in the memory map, Figure 11. The actual address locations of the Computer Program Components (CPC) are found in the assembly listing of the program (see Appendix D).

#### 5.4.4 Program Operation

The overall operation of the PBD software is shown in Figure 12.

#### 5.4.5 Assembly Constants

The assembly constants section of the source deck defines those constant values that are referenced symbolically throughout the source coding.

5.4.5.1 Accumulators--The programmable registers or accumulators in the CPU are referenced by the symbols AC0, AC1, AC2, and AC3.

<u>HEXIDECIMAL ADDRESS</u>	<u>CONTENTS</u>
0000 - 00FF	BASE PAGE (PROM)
1000 - 17FF	PBD SOFTWARE (PROM)
3000 - 32FF	DATA BASE (RAM)
3300 - 33FF	CCU (RAM)
EF00 - EFFF	CCU SOFTWARE (PROM)
FF00 - FFFF	TOP PAGE (PROM)

Figure 11. Memory Map of PBD  
Production Prototype  
Unit

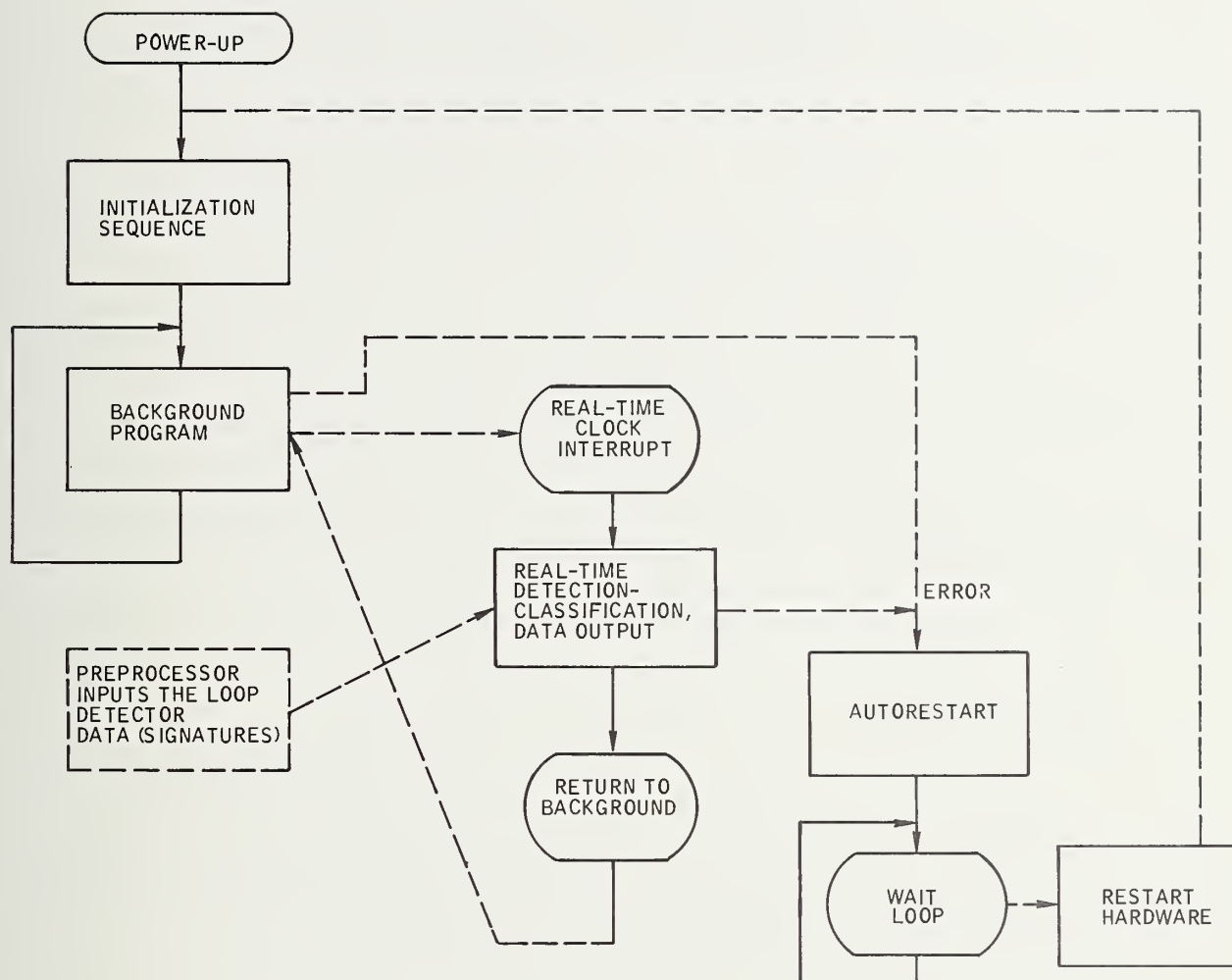


Figure 12. PBD Software Block Diagram

5.4.5.2 Input/Output Function Codes--These values are referenced in the operand field of input (RIN) and output (ROUT) instructions. The values are limited to seven bits.

5.4.5.3 Displacement Constants--These values are used in indexed addressing expressions and in bit displacement operands in the bit manipulation instructions.

5.4.5.4 Immediate Data Constants--These values are used in the operands of instructions using immediate data values.

5.4.5.5 Branch-On Condition (BOC) Codes--These jump condition symbols are used in the operands of the BOC instructions.

5.4.5.6 Control Flags--These symbols are used for referencing the processor control flags.

#### 5.4.6 Base Page CPC

The base page is the first 256 locations in memory. This page is directly addressable from anywhere in memory. Some base page locations are reserved for special purposes; the remaining locations are used for full-word constants and linkages to data and program entry points.

5.4.6.1 Reserved Locations--The following locations are reserved in the base page:

X'0000 - Jump-through pointer instruction for power-up.

X'0001 - Jump-through pointer instruction for general interrupt.



X'0002 - Reserved for system software use in the  
through software development system environment.  
X'001F

5.4.6.2 Program Entry Points--These data provide the address constants for accessing program entry points.

5.4.6.3 Data Base Pointers--These data provide the address constants for accessing data in the data base.

5.4.6.4 Common Constants--These full-word hexadecimal constants may be referenced by any instruction in memory.

5.4.6.5 Peripheral Device Address Constants--These data provide the constants that are loaded into AC3 in preparation for the input or output instruction which contains the seven-bit function codes. In the execution of the I/O instructions, the contents of AC3 are added to the seven-bit control field in the RIN or ROUT to obtain the peripheral device address and function code.

#### 5.4.7 Executive CPC

This CPC contains the executive functions for the PBD software. These functions include initialization, interrupt processing, self-testing, scheduling, output of bus/vehicle classifications, error recording, autorestart, and debug (CCU) service routines.

#### 5.4.7.1 Restart Initialization (ERSI)--

##### 5.4.7.1.1 Program Narrative--

- 1) Purpose--This routine performs the necessary software initialization sequences at power-up, after pressing the System Clear switch, or on autorestart.
- 2) Software Interfaces--This routine is entered via a jump-through pointer at memory location X'0000, which is reached by a jump-direct instruction at X'FFFE.

At initial power-up, for example, the PC is forced to X'FFFE to start this transfer sequence. This routine contains the following routines, some of which are described later:

ECCU	- CCU Initialization
EMAD	- RAM Test
EGIS	- Interrupt Servicing
ESCH	- RTC Scheduling
EADC	- Autorestart
XRTC	- Output Data
COTF	- Catch-on-the-Fly
EREO-7	- Error Recording

- 3) Assumptions--None.
- 4) Solution Approach--This routine controls the sequence that initializes memory and CCU, performs the RAM memory test, clears processor status

flags and stack, initializes the free-RAM entry point, starts the real-time clock (RTC), initiates the background test cycle, records any errors, and provides for debugging, interrupt handling, and (autorestart) restarting of the initialization cycle.

- 5) Program Operation--The stack-full condition is tested immediately to preclude an error on a subsequent subroutine call. The stack-full condition is an error and results in an autorestart being initiated provided the switch to permit this is in the ENABLE position. Next, the RTC is assured to be stopped, the RTC interrupt pulse is reset, and the general interrupt line is pulsed to disable interrupts. Then ECCU is called to initialize the CCU RAM and servicing routine.

Status flag 4 is cleared and the initial RAM test is performed by calling EMAD. Status flags 5, 6, 7 are reserved for expansibility. The first location in the RAM that is free for the insertion of patch code and is accessed by COTF is initialized with a standard return instruction. The CPU stack is initialized for the background programs, and the data base is cleared.

The Pseudo Halt Sense switch is tested and the program will loop at this instruction while the switch is on. After the switch is turned off, the RTC is started, background computations are initiated, and interrupts are enabled by the final return instruction.

- 6) Model--PBD33J.
- 7) Date--9 February 1977.
- 8) Remarks--None.

5.4.7.1.2 Program Work Areas--The initialization sequence controlled by this routine affects every location in RAM except the CCU RAM and five locations held in reserve. The RAM address test affects every location except the data base, the CCU RAM, and the five locations held in reserve. The entire data base area, including the bus detector signature data for the 16 detectors, is cleared to zero. Data base locations are then initialized as appropriate.

5.4.7.1.3 Program Flowchart--The program flowchart is represented in Figure 13.

5.4.7.1.4 Output Data Formats--The output control pulses issued by this routine are completely defined by the peripheral device address and function code. The contents of ACO are not used.

5.4.7.1.5 Report Formats--Not applicable.

5.4.7.1.6 Test Data--To be determined.

5.4.7.1.7 Revisions--None.

#### 5.4.7.2 General Interrupt Servicing Routine (EGIS)--

##### 5.4.7.2.1 Program Narrative--

- 1) Purpose--This routine services interrupts on the general interrupt line, and results in the real-time

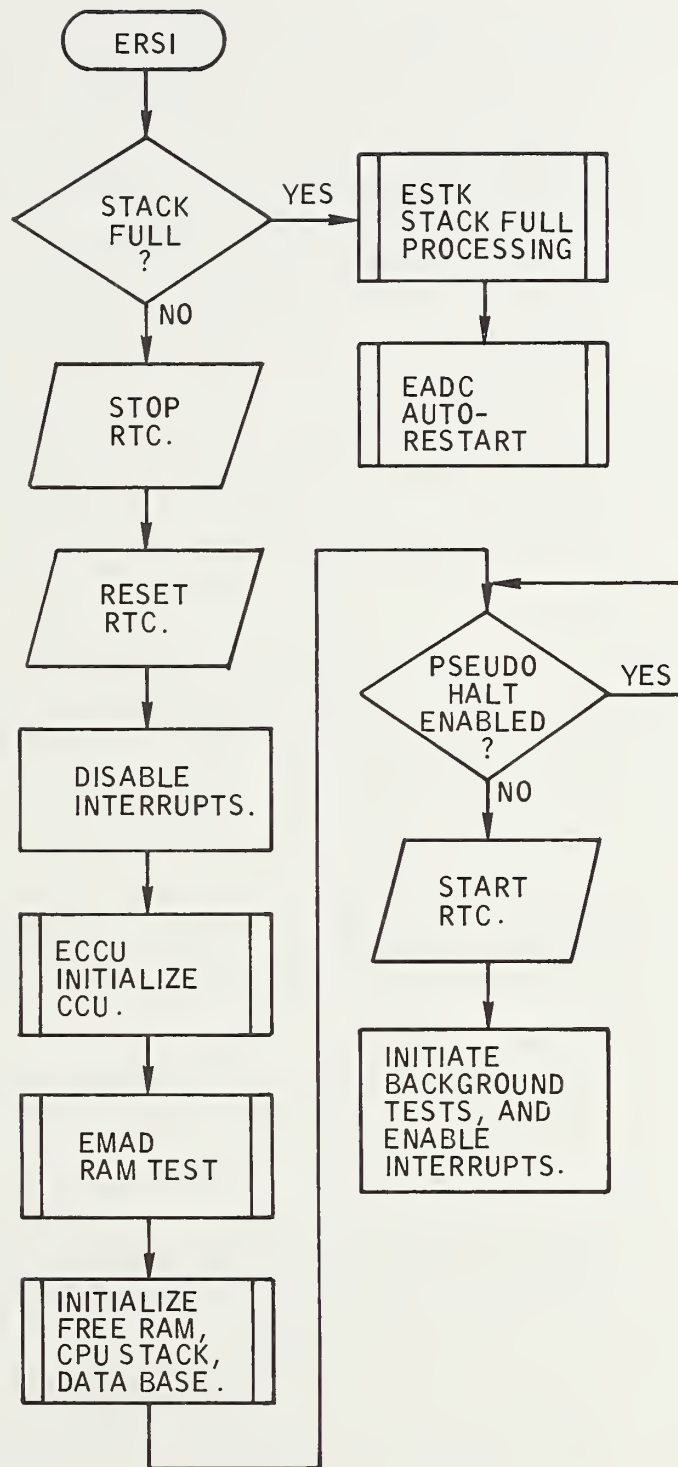


Figure 13. Restart Initialization Routine

detection-classification and data output of the results of the processing of vehicle signatures.

- 2) Software Interfaces--This routine is entered via the jump-through pointer instruction at memory location X'0001; it is reached as a result of the general interrupt forcing the program counter to X'0001.

In servicing the RTC interrupt, the Executive Scheduling routine, ESCH, is called to determine the order of processing vehicle signature data.

In the event of critical conditions which preclude further operation, the Autorestart routine, EADC, is called to allow reinitialization of the PDB system.

- 3) Assumptions--This routine is entered only as a result of the receipt of a general interrupt.

The stack-full and the RTC are the only sources of interrupts on the general interrupt line.

The stack-full processing routine at ESTK must be within PC relative addressing range of the BOC stack-full test instruction in ERSI.

The RTC compute flag is assumed to be in the first location in the executive data base at EBUF.



- 4) Solution Approach--On receipt of the general interrupt, the potential stack-full condition is tested for and, if necessary, serviced. Any stack-full error processing will result in the Autorestart routine (EADC) being called. To ensure a stack-full interrupt is generated and to prevent loss of data on a stack-full condition, two words of all 1's are loaded into the stack. The RTC compute flag is used to diagnose a clock error. A clock error indicates the failure to complete a previous interrupt sequence before the next one started and will result in the Autorestart routine (EADC) being called.
- 5) Program Operation--Since the receipt of an interrupt on the general interrupt line could be one of a stack-full condition, or from the RTC, the first condition tested for is the stack-full error. If the stack was found to be full, the error processing will result in the clearing of the stack-full condition and the saving of the computational environment (for possible diagnosis) and the entry of the Autorestart routine (EADC).

In the absence of the stack-full condition, normal processing will result in the saving of the computational environment and entry to the ERTC routine for additional interrupt processing.

In the ERTC routine, the RTC compute flag is tested and, if it is reset, normal processing continues, with the setting of the RTC complete flag, a call to the executive scheduler (ESCH), resetting the RTC compute flag on return from ESCH, and restoration of the computational environment followed by a return to the interrupted background program and enabling of interrupts.

- 6) Model--PBD33J.
- 7) Date--9 February 1977.
- 8) Remarks--None.
- 9) Program Work Areas--The computational environment at the time of an interrupt is saved in the RTC save area at ESAV or the stack-full area at ISV, as appropriate.

RTC clock error data are stored in the executive error buffer, EERR, and the RTC compute flag stored at EBUF in the executive data base.

5.4.7.2.3 Program Flowchart--The program flowchart is presented in Figure 14.

5.4.7.2.4 Output Data Formats--The output control pulse issued by this routine to stop the RTC is completely defined by the peripheral device address and function code. The data in ACO are not used.

5.4.7.2.5 Report Formats--Not applicable.

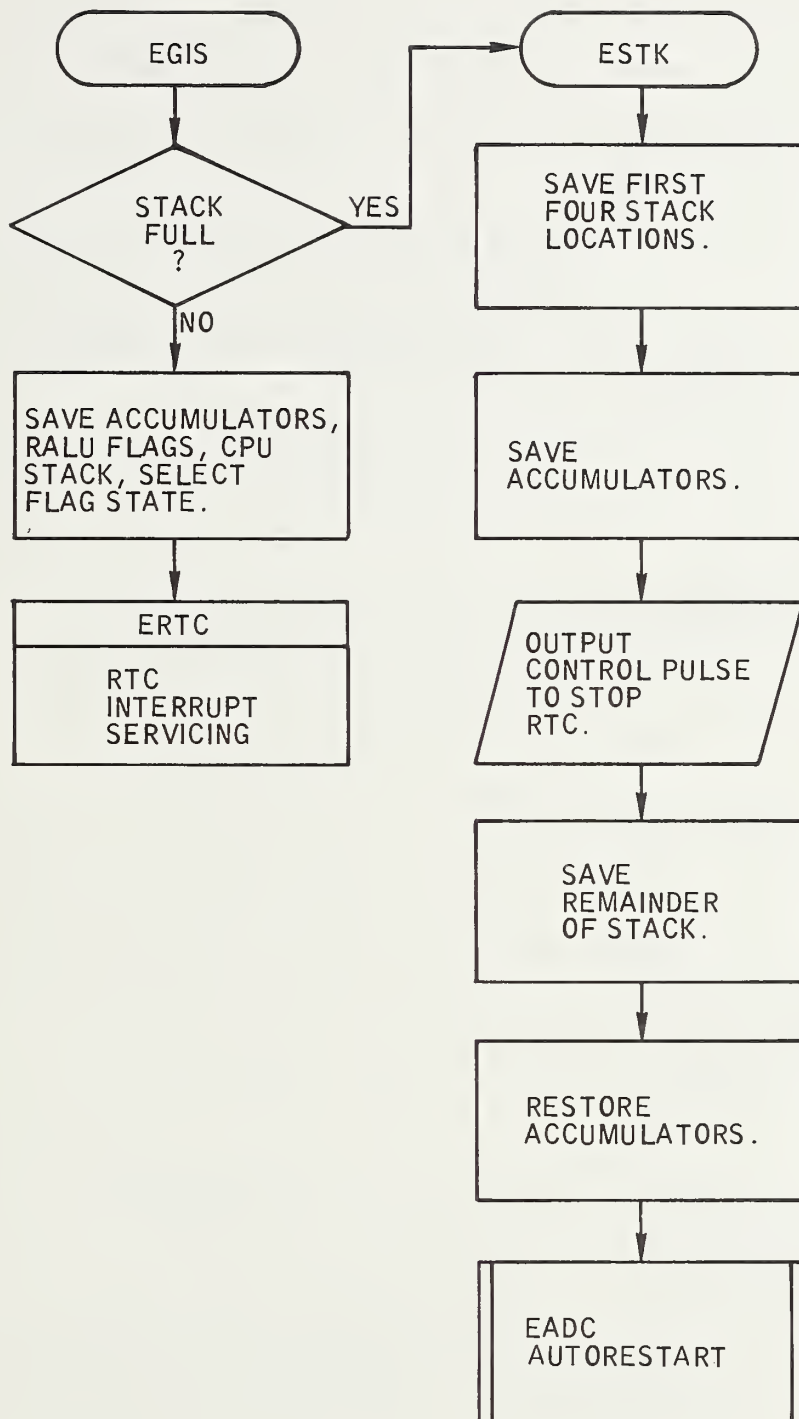


Figure 14. General Interrupt Service Routine  
(Executive CPC)

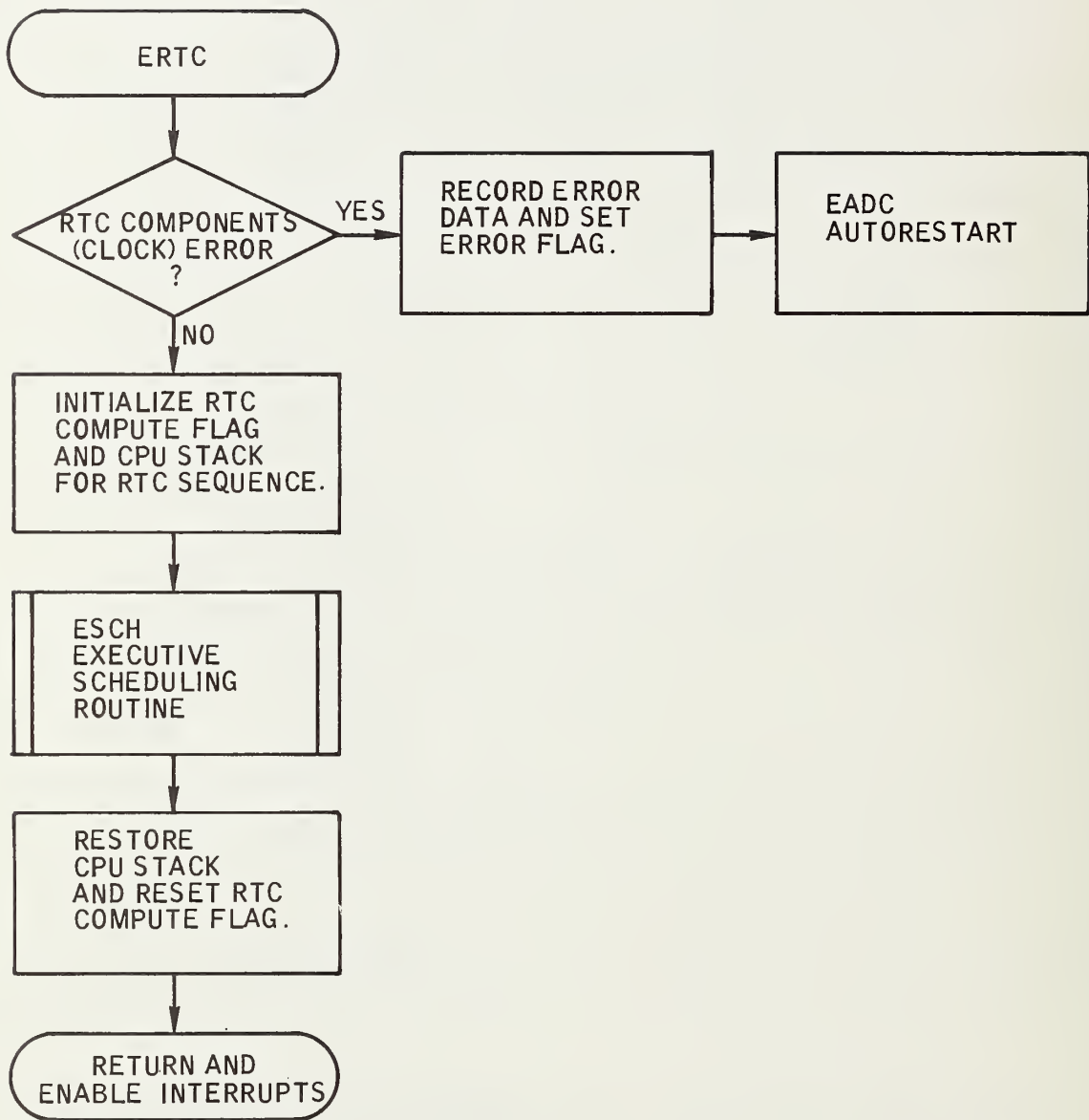


Figure 14. General Interrupt Service Routine (Executive CPC)  
(Concluded)

5.4.7.2.6 Test Data--To be determined.

5.4.7.2.7 Revisions--None.

5.4.7.3 Background Program Routine (EBKD)--

5.4.7.3.1 Program Narrative--

- 1) Purpose--This routine is the background program, a continuously looping RAM test, except during interrupt processing.
- 2) Software Interfaces--This routine is initiated by the return and enable interrupts instruction in ERSI at the end of the initialization sequence. This routine calls SMAD to perform the RAM test in real time. This routine continues to cycle until an error is detected, at which time this routine outputs a signal to light the Fault 1 light and enters EADC to initiate autorestart. When an interrupt is received during normal processing, this program will stop cycling until the return instruction in the interrupt handler is executed.
- 3) Assumptions--The RAM test is made in the unused area of memory from DEND+100 to X'32FF, the last location in free RAM. This is done to prevent a conflict between the PBD signatures and data base and CCU and debug program put in the COTF area.

Status flag 4 is assumed to be cleared prior to initiation of this routine and is set only by routine SMAD when a RAM test error is detected.

Also, the Fault 1 light, which lights when a RAM test error is detected, will not be reset by the software to allow maintenance personnel proper observation of this error condition.

- 4) Solution Approach--The starting and ending addresses of the test area are stored in the data base, a call to SMAD is made, with the return being to the error or no error location. If the status flag is set or if SMAD makes the error return path, the Fault 1 light will light and EADC, Autorestart, will be entered. If no error is detected, the program will loop on itself, testing and waiting for interrupts and the subsequent processing of real-time vehicle signature data. When interrupt processing is completed, a return will be made to the point at which this program was interrupted.
- 5) Program Operation--The program operation is as described in 3.3.3.1.4.
- 6) Model--PBD33J.
- 7) Date--9 February 1977.
- 8) Remarks--None.

5.4.7.3.2 Program Work Areas--The starting and ending addresses for the RAM test are stored in the data base locations SSAD and SEAD,



respectively. At the error return from SMAD, AC2 contains the erroneous contents of the address shown in AC3. These data are then saved in the Autorestart save area.

5.4.7.3.3 Program Flowchart--The program flowchart is shown in Figure 15.

5.4.7.3.4 Output Data Format--The Fault 1 light will light to indicate a RAM test error occurred. The failure data in AC2 and AC3 will be sent to EADC for saving in the data base for possible diagnostic use.

5.4.7.3.5 Report Formats--Not applicable.

5.4.7.3.6 Test Data--To be determined.

5.4.7.3.7 Revisions--None.

5.4.7.4 Autorestart (EADC)--

5.4.7.4.1 Program Narrative--

- 1) Purpose--This routine is entered when an error condition is detected by the software in response to critical conditions that preclude further system operation. When this routine finishes, and automatic hardware reset is normally applied to the system to cause a system restart.
- 2) Software Interfaces--This routine is called in response to the following conditions: a stack-full error, an RTC compute error, and RAM test errors.

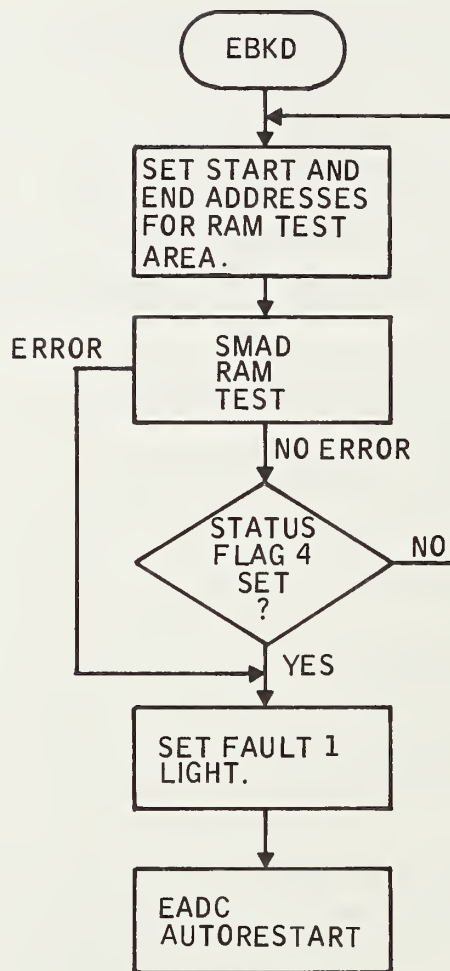


Figure 15. Background Program Routine (EBKD)

- 3) Assumptions--The Fault 2 light will not be reset by the software to allow operator observation of system operating characteristics. A switch is provided to reset the Fault 2 light, should it become necessary.

The switch to inhibit the hardware restart sequence shall have been set to the ENABLE position for an automatic restart. If left in the INHIBIT position, no further computations will take place.

- 4) Solution Approach--The computational environment at the time of entry to Autorestart (EADC) is saved for possible diagnostic evaluation purposes.

To examine the saved computational environment, it will have been necessary to have previously used the CCU (DANYL unit) to store a suitable program in the COTF area (to perhaps put some critical information in the five untouched locations after DEND) for later evaluation. This presupposes the error is repeatable and the CCU can then be attached for debug purposes.

It is possible to inhibit the hardware reset by use of the Disable switch. Then, if the Fault 2 light should come on, the program will stay in a terminal wait loop. The System Clear switch can then be used to restart the processor.

- 5) Program Operation--This routine saves the computational environment in the data base area and lights the Fault 2 light to signal maintenance personnel an error occurred. The software does not reset this Fault 2 light.

If it is desired to look at the error conditions caused an automatic restart, it will be necessary to enable the Inhibit switch to prevent an automatic system clear from occurring.

- 6) Model--PBD33J.

- 7) Date--9 February 1977.

- 8) Remarks--None.

5.4.7.4.2 Program Work Area--The computational environment that is saved in the data base will be zeroed if a system clear is initiated.

5.4.7.4.3 Program Flowchart--The program flowchart is shown in Figure 16.

5.4.7.4.4 Output Data--None.

5.4.7.4.5 Report Formats--Not applicable.

5.4.7.4.6 Test Data--To be determined.

5.4.7.4.7 Revisions--None.

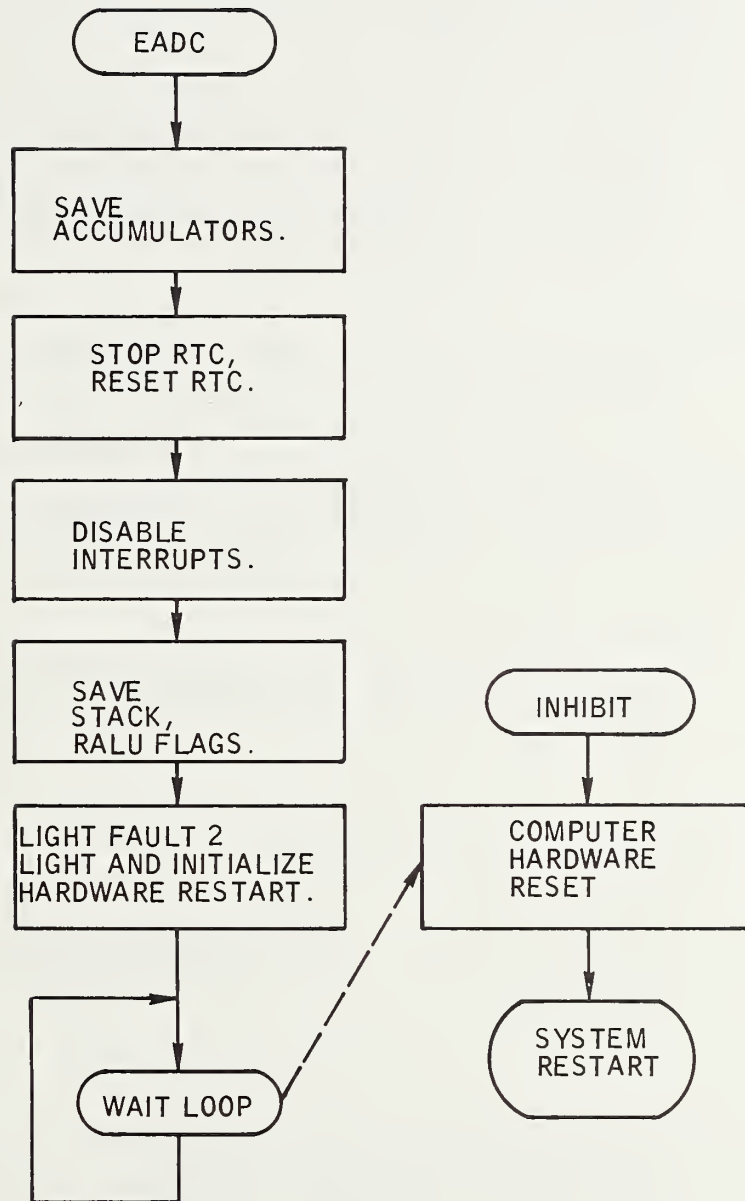


Figure 16. Autorestart (EADC)

#### 5.4.7.5 Executive Scheduling Routine (ESCH)--

##### 5.4.7.5.1 Program Narrative--

- 1) Purpose--Called as the result of an RTC interrupt, this routine calls the necessary subroutines to perform the real-time vehicle detection-classification sequences.
- 2) Software Interfaces--This routine is entered from the General Interrupt Servicing routine, EGIS. This routine calls COTF, Catch-on-the-Fly, if a switch is enabled, DMON, the Detector Monitor, and XRTC, to output the vehicle and bus data.
- 3) Assumptions--The RTC interrupt is reset prior to the instruction re-enabling interrupts being executed.
- 4) Solution Approach--This routine enables interrupts during the RTC sequence so that an RTC error may be detected. The ability to insert patch code, using the COTF routine, prior to the RTC sequence is provided.
- 5) Program Operation--The RTC interrupt is reset and general interrupts are enabled. The jump condition is tested for the conditional call to COTF. The RTC sequence (DMON, which calls VCLAS, and XRTC, which outputs classification data) is then executed. Finally, a return to the interrupted (EBKD) background program is made where execution continues until the next interrupt.



6) Model--PBD33J.

7) Date--9 February 1977.

8) Remarks--None.

5.4.7.5.2 Program Work Areas--Each called routine in the RTC sequence has its own work area assigned.

5.4.7.5.3 Program Flowchart--The program flowchart is shown in Figure 17.

5.4.7.5.4 Output Data Format--The output control pulse to reset the RTC interrupt pulse is completely defined by the function code and peripheral device address. The data in ACO is not used.

5.4.7.5.5 Report Formats--Not applicable.

5.4.7.5.6 Test Data--To be determined.

5.4.7.5.7 Revisions--None.

5.4.7.6 Detector Monitor (DMON)--

5.4.7.6.1 Program Narrative--

- 1) Purpose--This routine sequences through the signature data base, examining each of the 16 possible signatures for vehicle presence or bus/non-bus data. Two output words are updated each time through, one for vehicle presence and one for bus detected in any of 16 possible signatures.

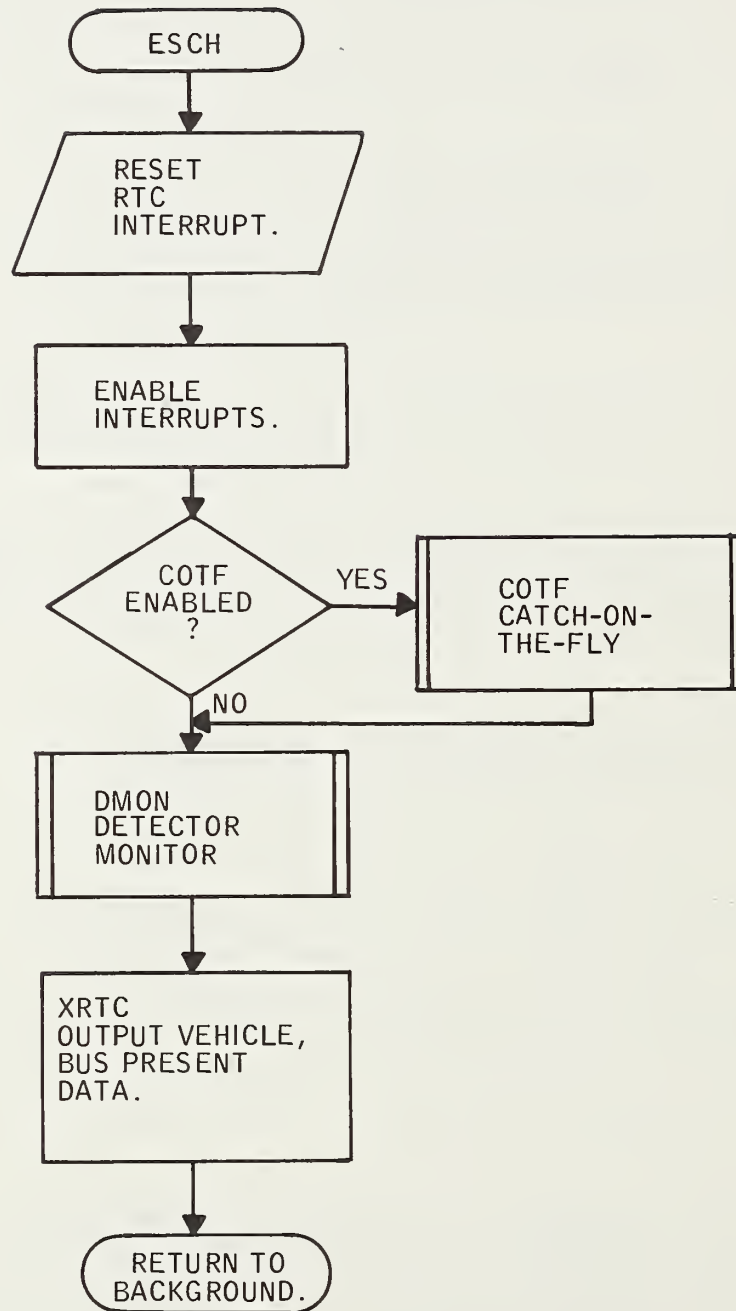


Figure 17. Executive Scheduling Routine (ESCH)

- 2) Software Interfaces--The Detector Monitor (DMON) routine is called by the Executive Scheduling routine (ESCH) in the Executive CPC. DMON calls VCLAS to examine a particular signature in the data base. The detector signature being examined is specified by a word (DCTR) in the data base.

The return from VCLAS to DMON is either to the next instruction following the call (via an RTS DO), indicating a vehicle signature in the data base was classified, or to the second instruction following the call (via an RTS DI), indicating no classification was made.

After returning from VCLAS, the vehicle presence bit for that DCTR is set or reset in the vehicle presence output word (VPREC), the bus bit is set or reset in the bus output word (BUSWD), and a return to the Executive Scheduling routine (ESCH) is made when all 16 detectors signatures have been examined.

- 3) Assumptions--The entry to DMON will be the ultimate result of the processor receipt of an interrupt that will arrive at a nominal time interval that permits, as a minimum, all detector monitor functions to be completed for all 16 detectors.

- 4) Solution Approach--The DMON routine maintains its own index counter (DCTR) to the particular detector signature data that it is processing.

DCTR is initialized to 1, processing takes place until vehicle presence (VPREC) and bus word (BUSWD) are established for this DCTR, then DCTR is incremented by 1 and processing is repeated. When DCTR reaches 16 and that detector's processing is completed, return is made to the scheduler (ESCH).

Each detector's signature may be examined once for each call to DMON. The vehicle presence bit in VPREC will be set or reset immediately when that detector's signature data indicates presence or nonpresence, respectively, of a vehicle. The bus word (BUSWD) bit for a given detector will be set immediately when a bus presence is detected, but will reset only after the bus bit set time delay (BUSSET) interval has expired.

The BUSSET interval is counted once each time through DMON, with each of the 16 detectors having its own counter in the data base.

Data for each of the 16 detectors are stored in VPREC and BISWD, each 16-bit words, so that the least-significant bit (LSB) represents detector 1 and the most-significant bit (MSB) represents detector 16.

- 5) Program Operation--DMON is called by ESCH once for each interrupt. The vehicle signatures

placed in the data base by the cycle steal hardware of the processor are examined as described in the operation paragraph; the vehicle presence (VPREC) and bus word (BUSWD) are formed and return is made to ESCH.

6) Model--None.

7) Date--9 February 1977.

8) Remarks--None.

5.4.7.6.2 Program Work Areas--All data are stored in the data base. Significant labels used are:

- DCTR - The current loop detector being examined runs from 1 to 16.
- DBIT - This table contains the mask bits used to locate/merge vehicle/bus data into the respective output words, VPREC, BUSWD.
- CLASS - Temporary location for bus/non-bus classification.
- CTR - Table of 16 counters, one for each output bit in BUSWD, used to lengthen any bus detected time interval.
- PRSNT - Vehicle presence data sent from VCLAS; each of the 16 detectors, in turn, uses this location.

5.4.7.6.3 Program Flowchart--The program flowchart is shown in Figure 18.

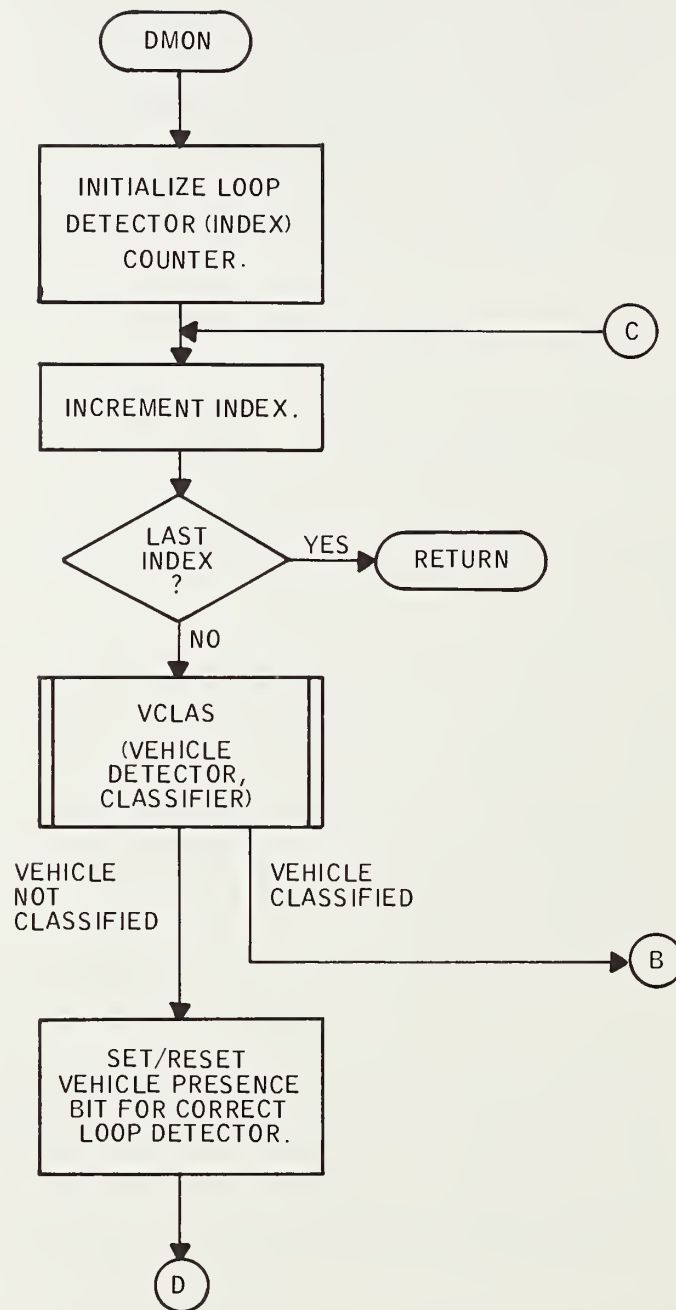


Figure 18. Detector Monitor Routine (DMON)



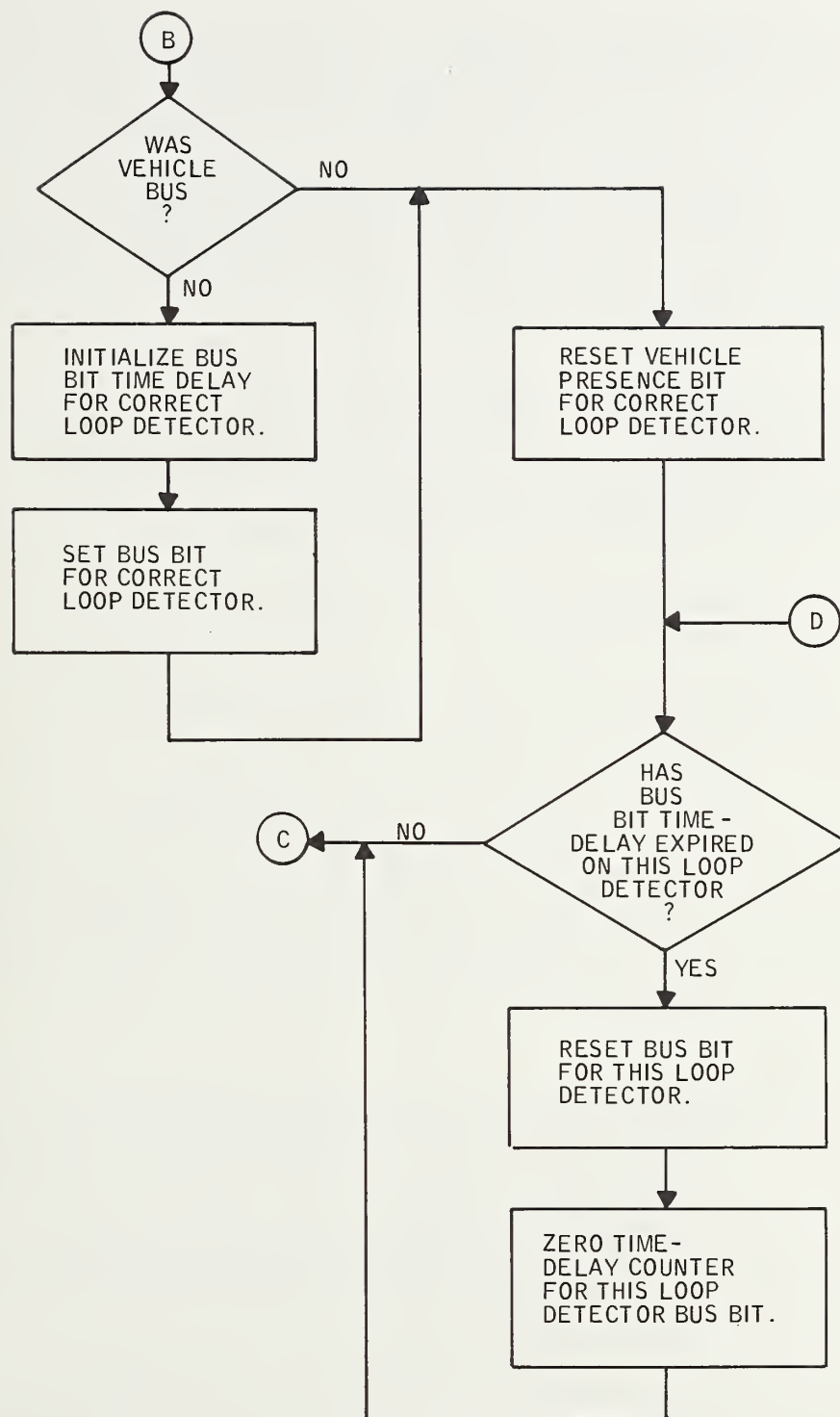


Figure 18. Detector Monitor Routine (DMON)  
(Concluded)

5.4.7.6.5 Output Data Format--The VPREC and BUSWD 16-bit words represent vehicle presence and bus-detected words, respectively, for each of the 16 possible detectors. The MSB (left-most) is 16 and the LSB (right-most) is 1 and correspond to the same number loop detector. When the particular bit is set ('1'), or reset ('0'), that indicates the presence or absence of a vehicle or bus, respectively. DMON stores VPREC and BUSWD for use by XRTC, the output routine.

5.4.7.6.6 Report Formats--Not applicable.

5.4.7.6.7 Test Data--To be determined.

5.4.7.6.8 Revisions--None.

5.4.7.7 Output Routine (XRTC)--

5.4.7.7.1 Program Narrative--

- 1) Purpose--This routine is called by the scheduler to output the vehicle presence (VPREC) and bus words (BUSWD) for each of the 16 possible detectors.
- 2) Software Interfaces--This routine is called by ESCH to output the data, VPREC, BUSWD, assembled by DMON. Enabling a test switch will permit the continuous outputting of '1's on these lines. They will return to the normal status when the switch is released.
- 3) Assumptions--The data in VPREC and BUSWD were prepared in DMON. The MSB (16) and the

remaining bits (15 through 1) correspond to the detector of the same number.

- 4) Solution Approach--Test for the test enable condition. If enabled, output two words of 1's in a loop until the test is disabled. If disabled, output VPREC and BUSWD.
- 5) Program Operation--The program operates as described in the Solution Approach and returns to the scheduler (ESCH) when done.
- 6) Model--PBD33J.
- 7) Date--9 February 1977.
- 8) Remarks--None.

5.4.7.7.2 Program Work Areas--The VPREC and BUSWD data base.

5.4.7.7.3 Program Flowchart--The program flowchart is shown in Figure 19.

5.4.7.7.4 Output Data Formats--The format is described in the assumptions paragraph.

5.4.7.7.5 Report Formats--Not applicable.

5.4.7.7.6 Test Data--To be determined.

5.4.7.7.7 Revisions--None.

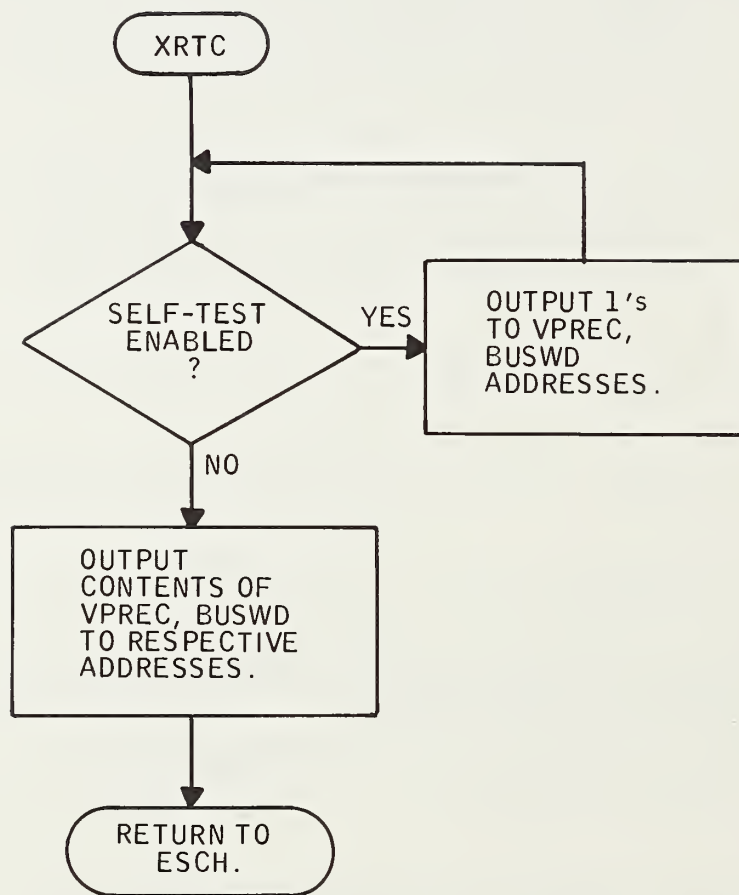


Figure 19. Output Data Routine (XRTC)

#### 5.4.7.8 Vehicle Classifier CPC (VC LAS)--

##### 5.4.7.8.1 Program Narrative--

- 1) Purpose--This routine determines vehicle presence on a given loop and later classifies the signature data as that of a standard 40-foot transit bus or not as a bus.
- 2) Software Interfaces--The Vehicle Classifier routine (VC LAS) is called by the Detector Monitor routine (DMON) to examine the data placed in the Signature Data Base (SDB) by a specific detector. The detector block to be examined is specified by DMON through a word in the data base (DC TR). The eighth word of the specified detector data base is first examined for the vehicle presence bit (bit 8, 0100 HEX). If this bit is set, a flag is stored in the data base (PRSNT) for use by DMON.

Secondly, the eighth word is examined for the presence of the end of signature bit (EOS, bit 1, 0001 HEX). If the EOS bit is reset (0000 HEX), a return to DMON is made via an RTS D1 instruction (indicating no classification was attempted by VC LAS).

If the EOS bit is set, the VC LAS routine continues to process the data sorted in the signature data base (VCDB) and will classify it as a bus or non-bus. If the vehicle is a bus, ACO is set to zero

(otherwise, ACO is set to 1) and a return to DMON is made via an RTS DO instruction (indicating a vehicle was classified by VCLAS).

- 3) Assumptions -- The Vehicle classifier is concerned with distinguishing between "standard transit" busses and other vehicles (non-busses).
- 4) Solution Approach -- VCLAS is given a loop detector index pointer (DCTR) to a segment of the SDB that contains the vehicle signature data items gathered by a specific detectors cycle steal/memory access hardware. VCLAS decides whether the data items meet the required criteria, whether the vehicle should be evaluated by the moving or stopped vehicle classifier, and whether the vehicle is a bus or non-bus. If an error is detected, the incident is recorded in PERR by the Proper Error handling routine. VCLAS will either return to DMON without classifying the data, or will return with the data indicating the vehicle was a bus or non-bus.
- 5) Program Operation -- VCLAS operates as described above when called by DMON to examine a given SDB segment. In addition, after the EOS bit is detected, the vehicle signature data items (eight words) are copied to VCDB to allow processing to take place without interruption due to possible changing conditions.



Following the copy operation, word 8 is examined to see if EOS is still set. If word 8 has not changed, or if it has changed but the third peak amplitude value is greater than zero, VCLAS continues to classify and return to DMON will be via an RTS DO.

During classification, the data items are examined to ensure that range, data order, and gross feature criteria are met. If these restrictions are not met, the errors detected are recorded by PERR and return to DMON will be via an RTS DI. If the restrictions are satisfied, an initial evaluation determines whether the "stopped" or "moving" vehicle classification algorithm should be used. The results of classification as a bus, ACO=0, or non-bus, ACO=1, are sent to DMON via an RTS DO.

Additionally, the cycle steal/preprocessor hardware that puts data in the SDB, will indicate the start of a new vehicle signature datum in the SDB by zeroing the sixth and eighth words. It is these changing conditions that are referred to above. If, following the copy described above, these words are found to be zero, classification does not take place and return to DMON is via an RTS D1.

- 6) Model -- PDB33J.
- 7) Date -- 9 February 1977.
- 8) Remarks -- None.

5.4.7.8.2 Program Work Areas -- The following data are stored in the data base:

1) Counters and Accumulators --

VCVC(32) - Vehicle Classifier Vehicle Counter array with one word reserved for each detector. Used for detector failure monitoring. Value stored within a word is incremented when the corresponding detector has placed a valid vehicle signature in SDB.

VCLOG(12) - First word of the Vehicle Classifier Vehicle Log. Statistics such as number of busses, non-busses, moving vehicles, and stopped vehicles are recorded here. Located in data base, these counters are for all vehicles, all detectors, and are limited to less than  $2^{16}$ .

VCLOG and VCLOG + 1 - A double-precision word containing the number of signatures rejected as noise.

VCLOG + 2 and VCLOG + 3 - A double-precision word containing the number of signatures that failed the gross features test.

VCLOG + 4 and VCLOG + 5 - A double-precision word containing the number of signatures that were handled by the stopped vehicle classifier.

VCLOG + 6 and VCLOG + 7 - A double-precision word containing the number of signatures that were handled by the moving vehicle classifier.

VCLOG + 8 and VCLOG + 9 - A double-precision word containing the number of signatures classified as busses.

VCLOG + 10 and VCLOG + 11 - A double-precision word containing the number of signatures classified as non-busses.

PERR(17) - VCLAS Error Buffer.

PERR(1) - Error Flag.

PERR(2) - Number of overflow errors detected.

PERR(3) - Specified detector during last overflow error.

PERR(4) - Number of times specified detector was out of range.

PERR(5) - Specified detector during last such error.

PERR(6) - Number of times an amplitude value was out of range.

- PERR(7) - Specified detector during last such error.
- PERR(8) - Number of times a time value was out of range.
- PERR(9) - Specified detector during last such error.
- PERR(10) - Number of times a time value was out of sequence.
- PERR(11) - Specified detector during last such error.
- PERR(12) - Number of vehicle signatures rejected as noise.
- PERR(13) - Specified detector during last such error.
- PERR(14) - Number of times EOS status word changed during copy operation.
- PERR(15) - Specified detector during last such error.
- PERR(16) - Number of times a signature was lost during a copy operation.
- PERR(17) - Specified detector during last such error.

## 2) Hold Areas --

- VCDB(16) - Vehicle Classifier Data Base. This array in the data base contains information used and produced by the vehicle classifier routine.

DCTR - Detector index number specifies which detector data block is to be examined by VCLAS. Located in data base.

SDB(16, 8) - Signature data block contains all detector data blocks.

3) Vehicle Presence --

PRSNT - Set to '1' if a detectors word 8, bit 8, is set, or to '0' if bit 8 is reset.

4) Detector Index Range (1 to 16) --

VCHD - Highest detector index number (DCTR) expected.

VCLD - Lowest detector index number -1.

5) Masks --

VCMA - Mask used in amplitude in-range test.

VCMT - Mask used in time in-range test.

VCMOF - Mask used in time overflow test.

6) Constants Used in Moving/Stopped Test --

VCST1 - Evaluation term for  $F1 + F2$ .

VCST2 - Evaluation term for  $F0$  (lower bound for moving vehicle).

VCST3 - Evaluation term for  $F0$  (upper bound for moving vehicle).

7) Constants Used in Stopped Vehicle Classifier --

VC31	- G1 coefficient for H1 function.
VC32	- G2 coefficient for H1 function.
VC41	- G1 coefficient for H2 function.
VC42	- G2 coefficient for H2 function.
H1 T1	- Evaluation term for H1 function (lower bound for bus).
H1 T2	- Evaluation term for H1 function (upper bound for bus).
H2 T1	- Evaluation term for H2 function (lower bound for bus).
H2 T2	- Evaluation term for H2 function (upper bound for bus).
VCM15	- Mask used for double precision comparisons.
VCCO	- Term for clearing overflow status bit.
VCCO+1	- F1 coefficient for K4.
VCCO+2	- F2 coefficient for K4.
VCCO+3	- G1 coefficient for K4.



VCCO+5	-	K4 Bias (residue).
VCCO+6	-	F1 coefficient for K5.
VCCO+7	-	F2 coefficient for K5.
VCCO+8	-	G1 coefficient for K5.
VCCO+9	-	G2 coefficient for K5.
VCCO+10	-	K5 Bias (residue).

5.4.7.8.3 Program Flowchart -- The program flowchart is presented in Figure 20.

5.4.7.8.4 Output Data Formats -- Not applicable.

5.4.7.8.5 Report Formats -- Not applicable.

5.4.7.8.6 Test Data -- To be determined.

5.4.7.8.7 Revisions -- None.

5.4.3.9 Initialize Computer Control Unit Routine (ECCU)--

5.4.7.9.1 Program Narrative --

- 1) Purpose -- This routine initializes the RAM data base for the CCU (DAYNL Unit) and makes the initial entry into the CCU servicing routine.

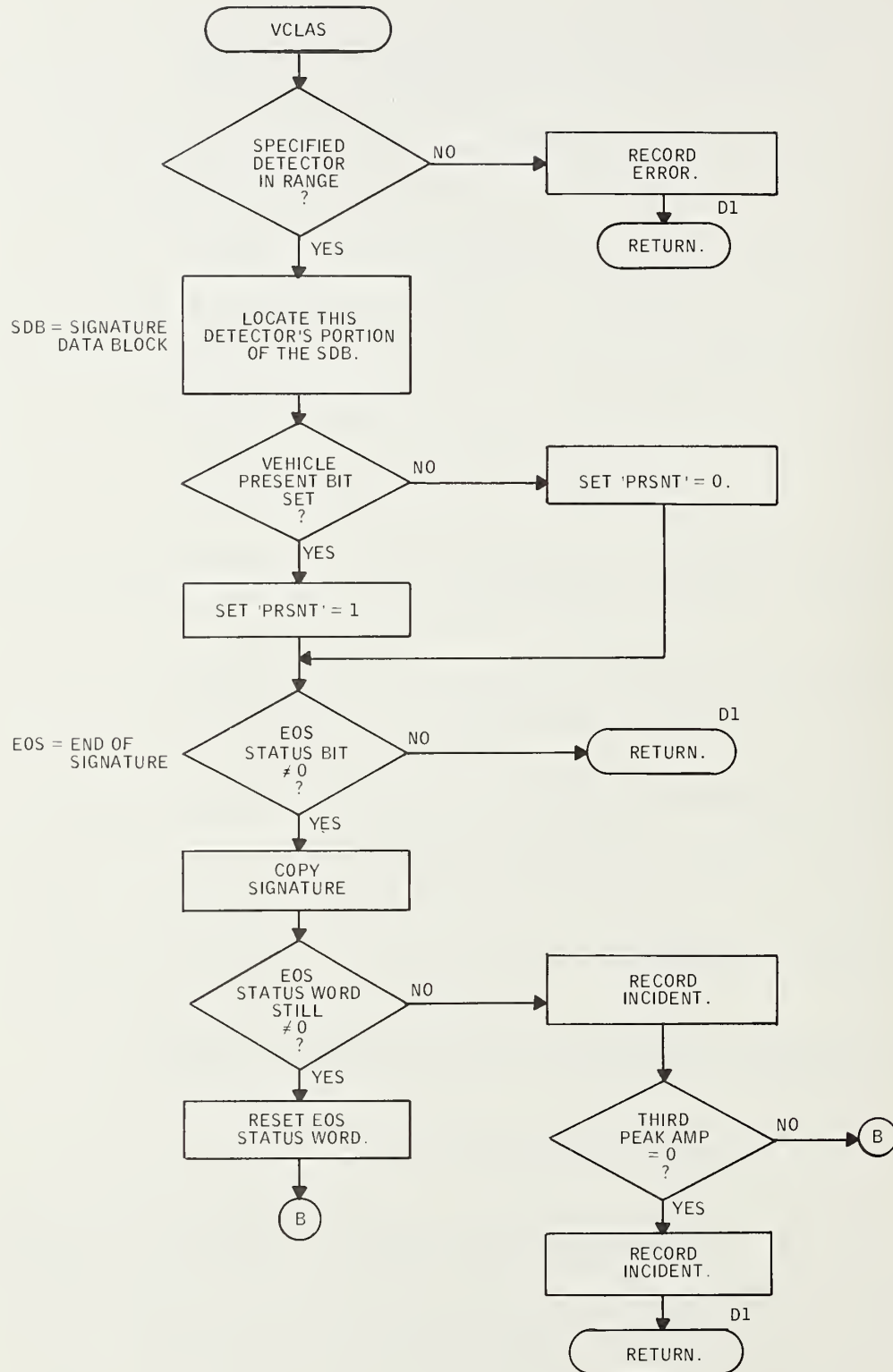


Figure 20. Vehicle Classification Routine (VCLAS)

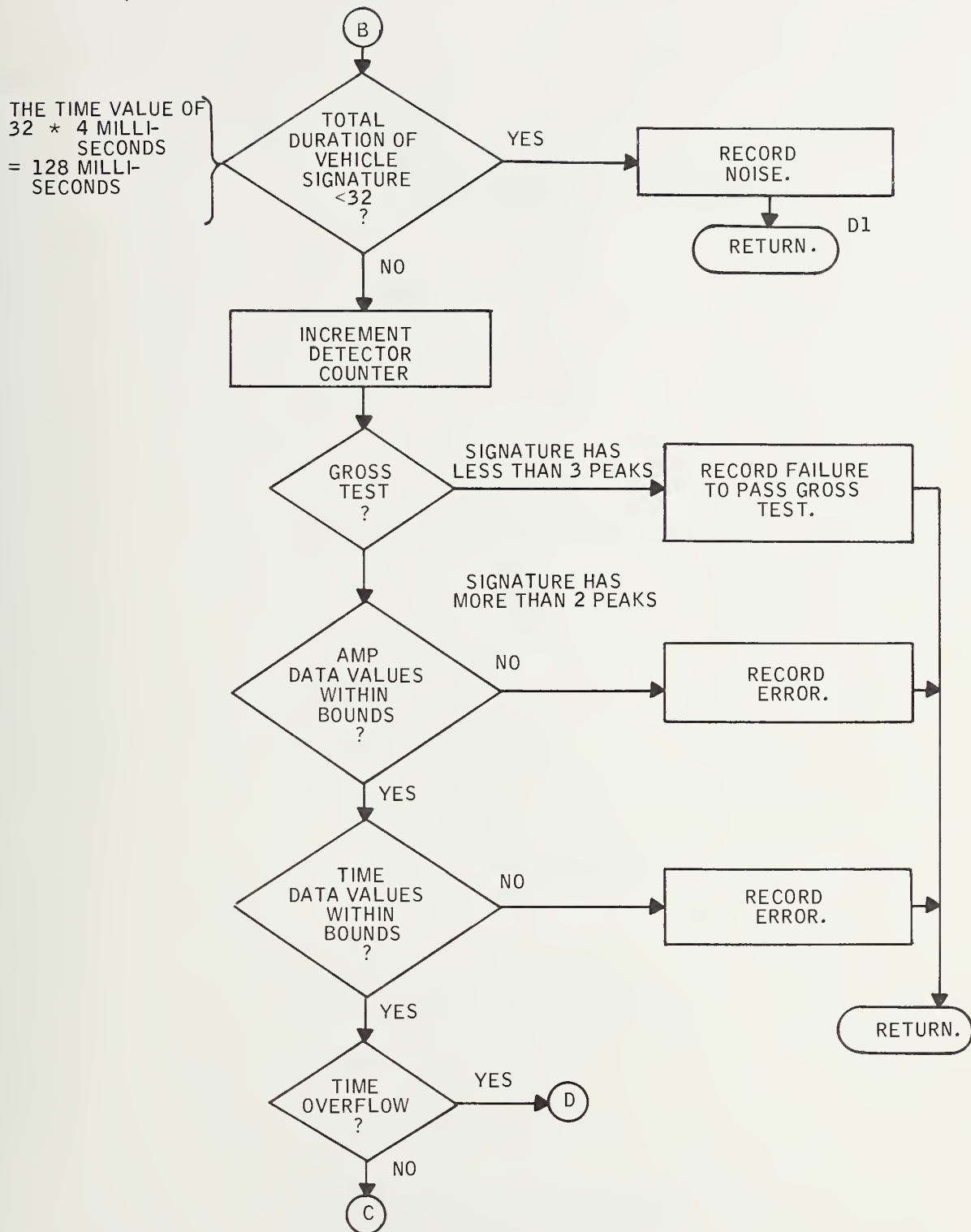


Figure 20. Vehicle Classification Routine (VC LAS) (Continued)

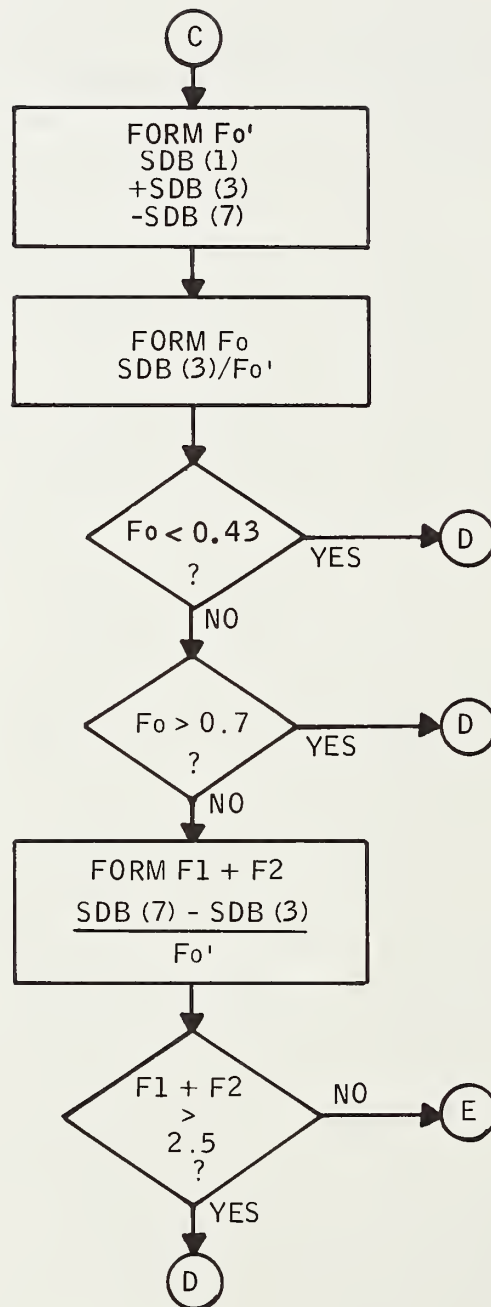


Figure 20. Vehicle Classification Routine (VCLAS) (Continued)

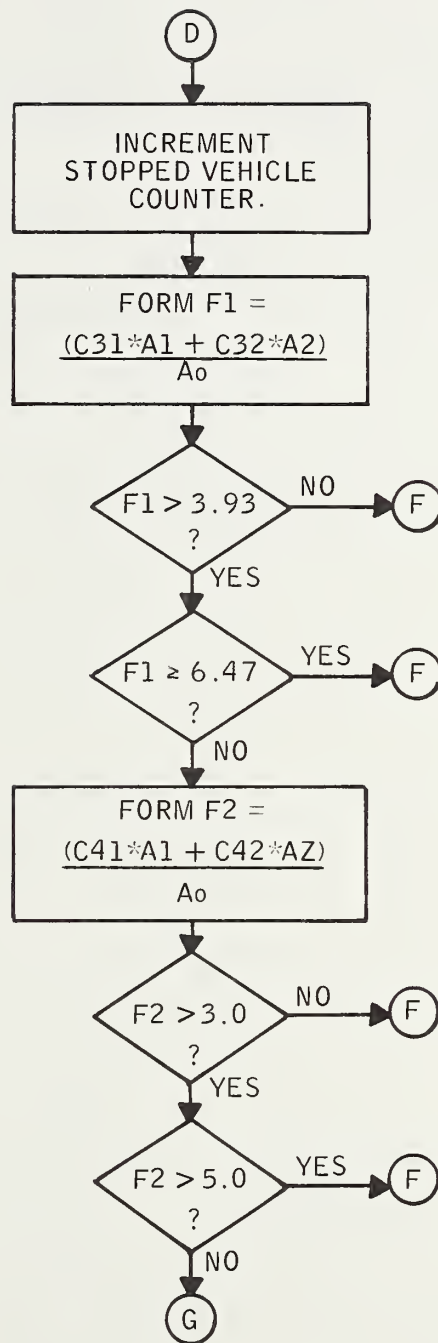


Figure 20. Vehicle Classification Routine (VCLAS) (Continued)

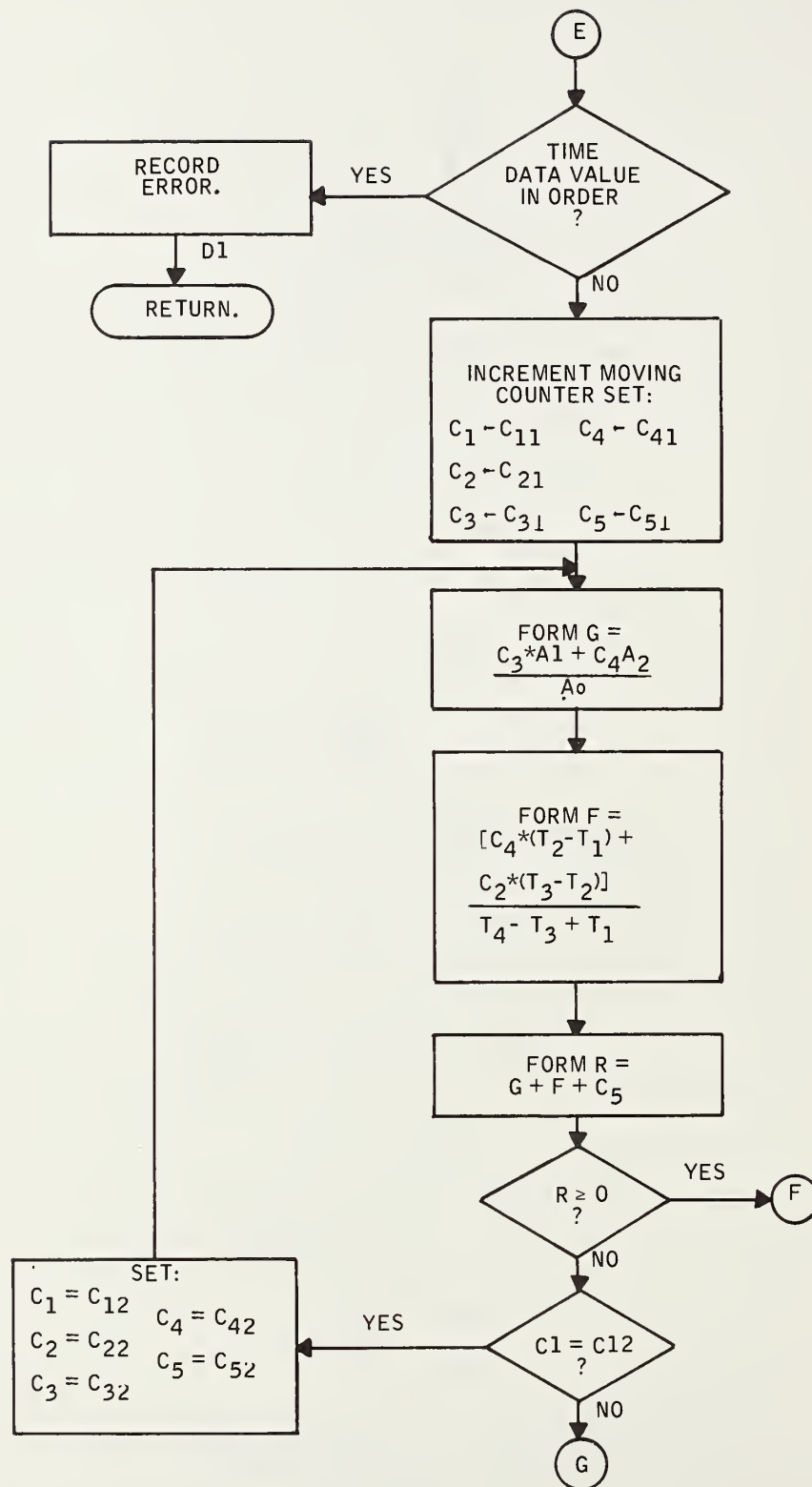


Figure 20. Vehicle Classification Routine (VC LAS)  
(Continued)



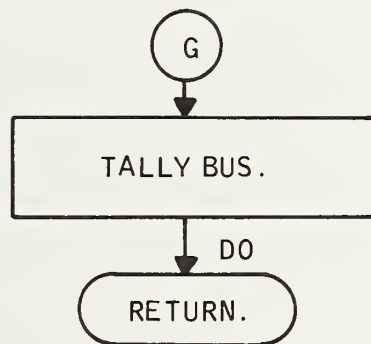
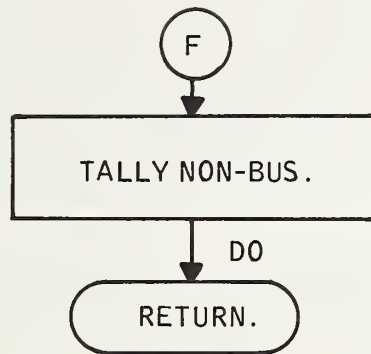


Figure 20. Vehicle  
Classification  
Routine (VCLAS)  
(Concluded)

- 2) Software Interfaces -- This routine is called only during the initialization sequence from ERSI. This routine makes the initial entry to the CCU servicing routine. This routine initializes the RAM data base for the CCU.
- 3) Assumptions -- The CCU servicing is assumed to be located at X'EF00 and to begin with the instruction value X'86F7. The CCU data base is assumed to be located in the 48 words starting at address X'33D0.
- 4) Solution Approach -- Tests are made prior to any initialization functions to assure that the CCU is in the system. If the tests indicate that the CCU is not in the system, a return to the calling program is taken immediately.
- 5) Program Operation -- Jump condition X'C is tested with the BOC instruction to test for the CCU in the system. If the jump condition is true, then an additional test on the CCU servicing routine is made. The first instruction is accessed and compared with the local data value. If the instruction agrees, then initialization continues.

The CCU RAM is first cleared to all zeroes. Then the state word is set to 1 and the two breakpoint addresses are set to -1. The return address is initialized to the location of the RTS instruction in this routine, the PUSH/PULL pointer is set to the first location in the RAM work area, and AC0 is set to 0 for the initial display on the CCU. The CCU routine is then entered via a jump-through pointer to preclude a stack entry,

as the return will be made to the address previously stored in the CCU data base.

6) Model -- PBD33J.

7) Date -- 9 February 1977.

8) Remarks -- This routine must interface with the CCU servicing routine that is supplied with that device.

5.4.7.9.2 Program Work Areas -- This routine initializes the RAM data base provided for the CCU.

5.4.7.9.3 Program Flowchart -- The program flowchart is presented in Figure 21.

5.4.7.9.4 Input/Output Data Formats -- Not applicable.

5.4.7.9.5 Report Formats -- Not applicable.

5.4.7.9.6 Test Data -- To be determined.

5.4.7.9.7 Revisions -- None.

5.4.7.10 Initialization RAM Address Test Monitor Routine (EMAD) --

5.4.7.10.1 Program Narrative --

1) Purpose -- This routine monitors the RAM tests performed during the initialization sequence.

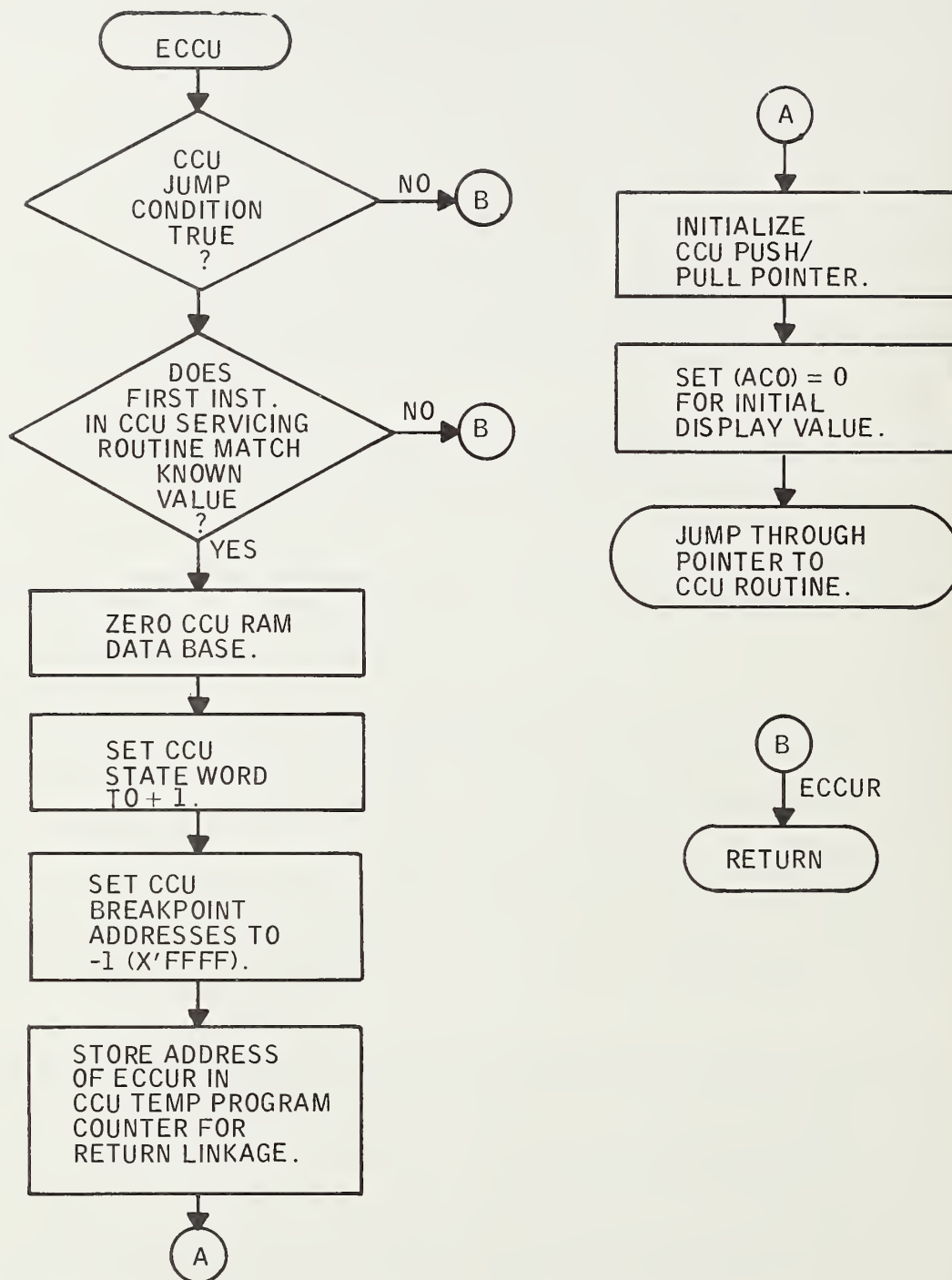


Figure 21. Initialize Computer Control Routine (ECCU)

- 2) Software Interfaces -- This routine is called only by the restart initialization routine, ERSI. This routine calls SMAD to test each block of RAM available for testing. In the event of error, the Autorestart routine, EADC, is called. Hexadecimal constants from the base page are referenced to establish the start and end addresses for the tests.
- 3) Assumptions -- The end of the data base is assumed to be just prior to ADEND. The CCU RAM is assumed to be in the range X'33D0 to X'33FF. The no error return from SMAD is at a nonstandard return displacement of 1 and the error return at the standard displacement of 0.
- 4) Solution Approach -- The RAM containing the data base is tested from just beyond the data base (ADEND) to the end of the available RAM.
- 5) Program Operation -- The RAM containing the data base is tested over the unused locations. An error results in an automatic restart.
- 6) Model -- PBD33J.
- 7) Date -- 9 February 1977.
- 8) Remarks -- None

5.4.7.10.2 Program Work Areas -- This routine initializes the start and end address data for the RAM address test routine in data base locations SSAD and SEAD, respectively.

- 5.4.7.10.3 Program Flowchart -- The program flowchart is presented in Figure 22.
- 5.4.7.10.4 Input/Output Data Formats -- Not applicable.
- 5.4.7.10.5 Report Formats -- Not applicable.
- 5.4.7.10.6 Test Data -- To be determined.
- 5.4.7.10.7 Revisions -- None.
- 5.4.7.11 RAM Address Test Routine (SMAD) --
- 5.4.7.11.1 Program Narrative --
- 1) Purpose -- This routine performs a test on a block of consecutive addresses in RAM.
  - 2) Software Interfaces -- This routine is called by EMAD during initialization and is called by EBKD during each cycle through the background computations. The start and end addresses for the test are accessed in the data base.
  - 3) Assumptions -- The block of addresses are assumed to be in RAM. The start and end addresses are assumed to be loaded into the data base prior to entry to this routine.
  - 4) Solution Approach -- Each location in the free-RAM address block is tested. Two consecutive errors at the same location are required for stopping the test



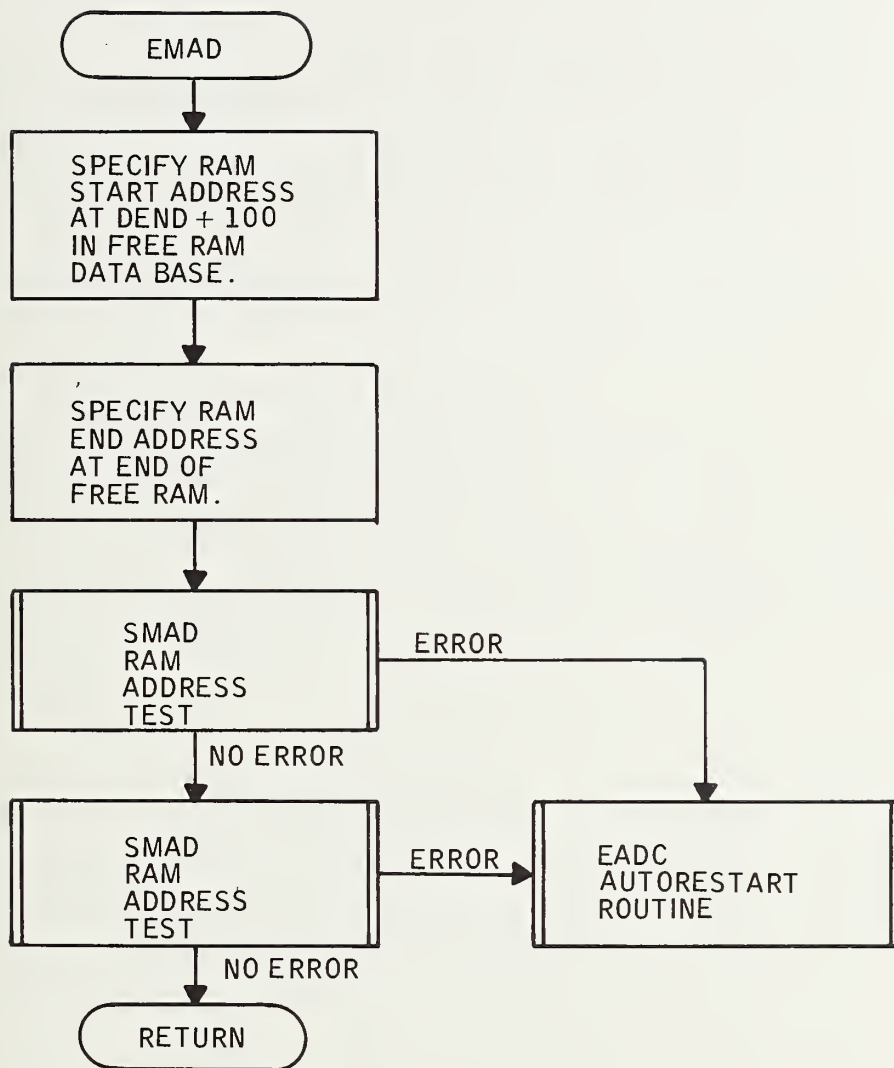


Figure 22. Initialization RAM Address Test Monitor Routine (Executive CPC)

and taking the error exit. The no-error condition is indicated by a nonstandard return with a displacement of 1. The error return is a call to Autorestart (EADC) after the Fault 1 light is lit.

- 5) Program Operation -- The address value is stored at each location in the specified block of addresses. The contents of each location are then accessed and compared with the address. The first mismatch at a location results in a retry. If the retry also fails, the error exit is taken.

At the error exit, the erroneous contents are loaded into AC2, the address remains in AC3, and CPU status flag 4 is set, and Fault 1 light is lit.

- 6) Model -- PBD33J.

- 7) Date -- 9 February 1977.

- 8) Remarks -- For a RAM consisting of discrete parts which provide 1 bit in each memory word over some address range, the address at which this test fails should indicate the bad part. The Fault 1 light is not reset by software.

5.4.7.11.2      Program Work Areas -- The start and end address for the test are found in SSAD and SEAD, respectively. AC0 is used as the consecutive failure counter. CPU status flag 4 is set for an error.

5.4.7.11.3 Program Flowchart -- The program flowchart is presented in Figure 23.

5.4.7.11.4 Output Data Formats -- Not applicable.

5.4.7.11.5 Report Formats -- Not applicable.

5.4.7.11.6 Test Data -- To be determined.

5.4.7.11.7 Revisions -- None.

5.4.7.12 Catch-on-the Fly Routine (COTF) --

5.4.7.12.1 Program Narrative --

- 1) Purpose -- This routine provides a COTF capability for programs executing in the RTC interrupt environment.
- 2) Software Interfaces -- This routine is called by the Executive Scheduling routine (ESCH), conditional upon the jump conditions X'E as tested by the BOC instruction. This routine transfers control to the first location in free RAM where patch code may be entered via the CCU.
- 3) Assumptions -- The RTC is assumed to be running at entry to this routine and is restarted prior to exit from this routine. The RAM patch code is assumed to make a standard return to this routine.

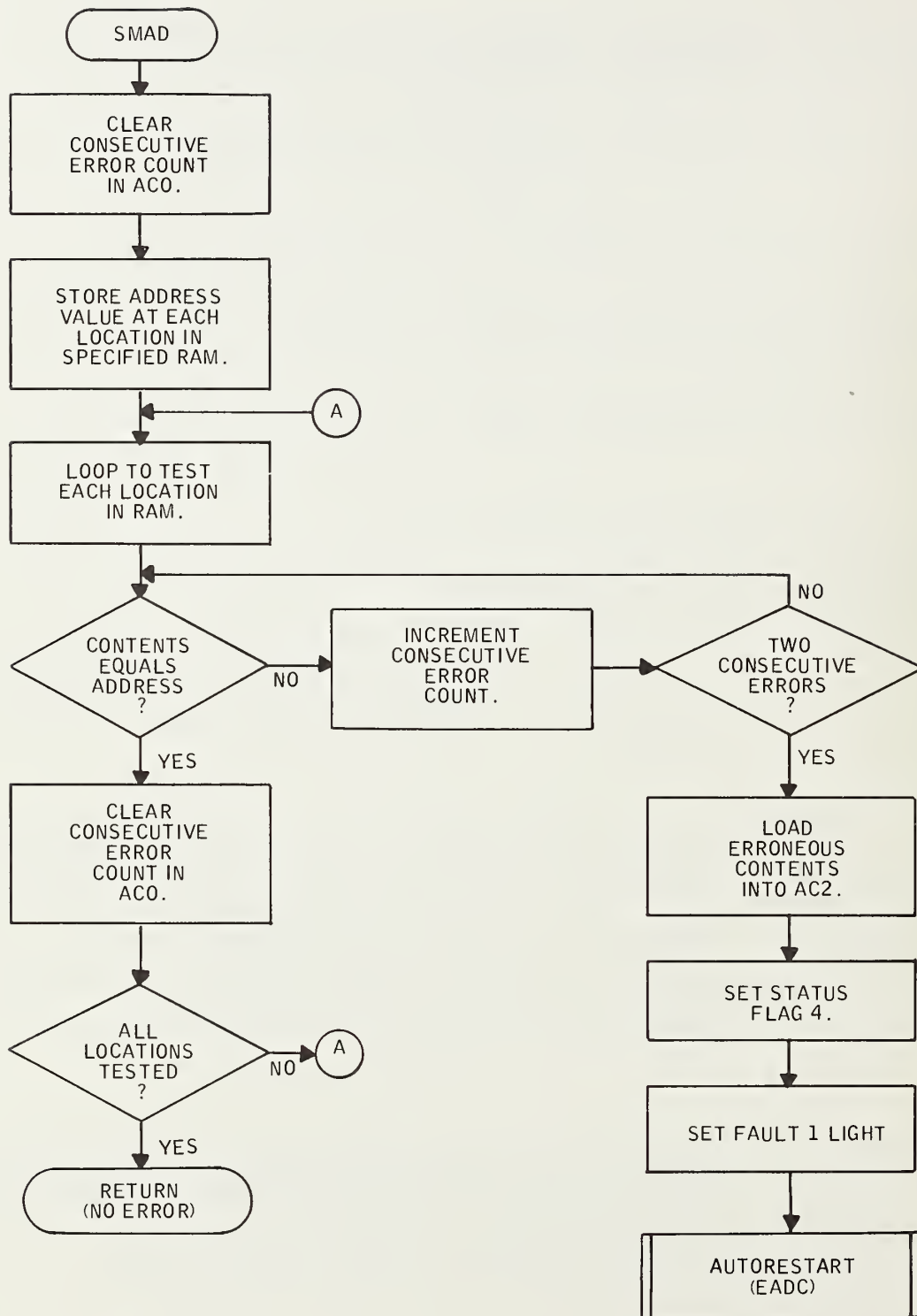


Figure 23. RAM Address Test Routine (SMAD)

- 4) Solution Approach -- The computational environment is saved, the RTC disabled, and control transferred to the first location in the free RAM. Following return, the clock is restarted and the environment is restored. Interrupts are not enabled or disabled by this routine.
- 5) Program Operation -- The accumulators, RALU status flags, stack, and select flag are saved. The RTC is stopped and the interrupt pulse assured to be reset. The transfer is made to the free RAM. The clock is then started and the computational environment restored.
- 6) Model -- PBD33J.
- 7) Date -- 9 February 1977.
- 8) Remarks -- For COTF operation in a RAM, locations are reserved by NOP instructions for patching or for the insertion of HALT or SNAP operations with the Debut routine in the IMP-16P.

5.4.7.12.2 Program Work Areas -- The computational environment is saved in the COTE save area, CSAV, in the data base.

5.4.7.12.3 Program Flowchart -- The program flowchart is presented in Figure 24.

5.4.7.12.4 Output Data Formats -- The output control pulses issued by this routine are completely defined by the peripheral device address and function code and are not dependent on the contents of accumulator 0.

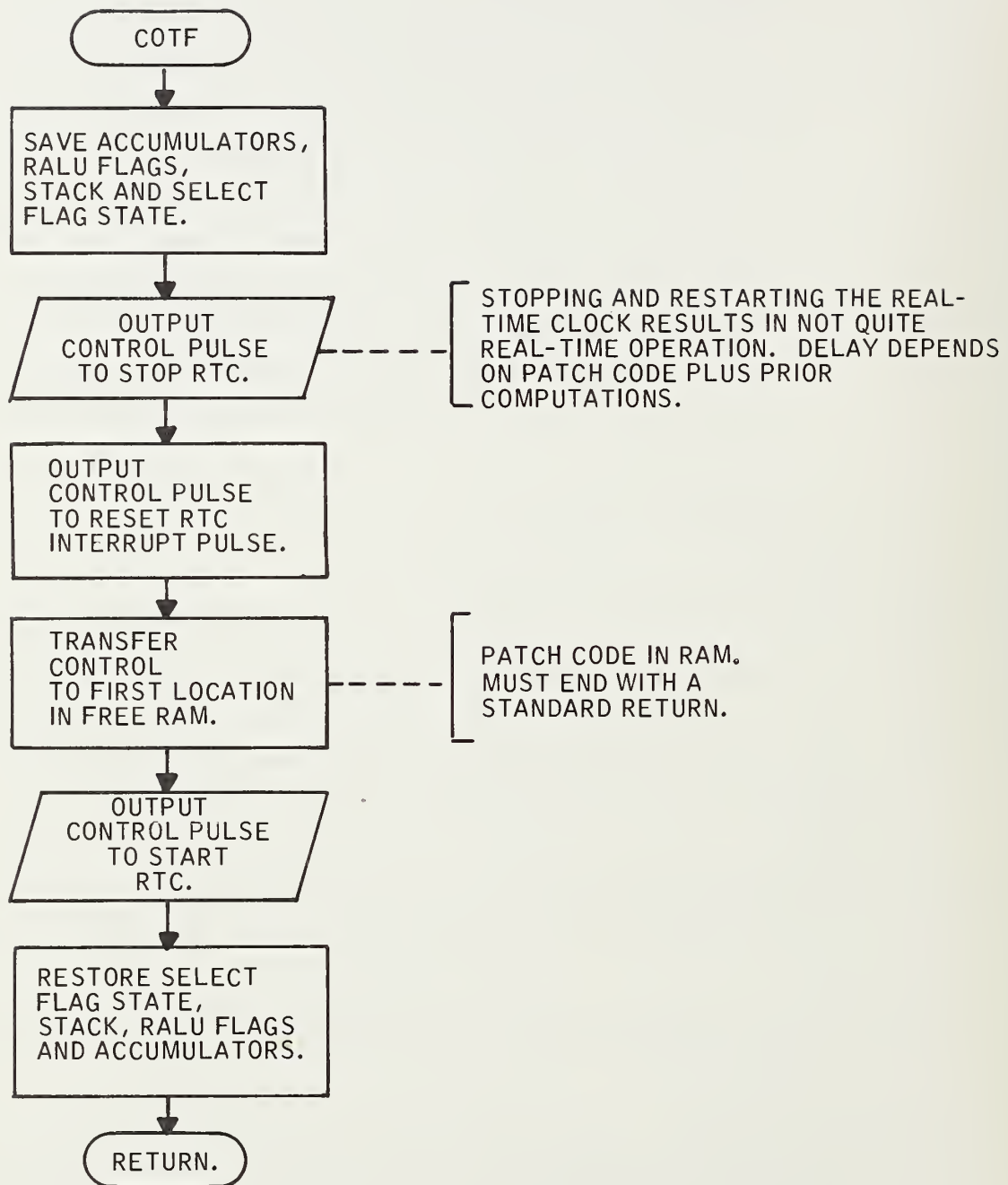


Figure 24. Catch-on-the-Fly Routine (COTF)



5.4.7.12.5 Report Formats--Not applicable.

5.4.7.12.6 Test Data--To be determined.

5.4.7.12.7 Revisions--None.

#### 5.4.8 Data Base

The data base consists of the signature data for the bus classification detectors and the data base for each Computer Program Component (CPC).

5.4.8.1 Bus Detector Signature Data (VCSDB)--The signature data block for each detector consists of eight values in the following sequence:

- 1) Total duration of signature
- 2) Amplitude of first peak
- 3) Time of first peak
- 4) Amplitude of second peak
- 5) Time of second peak
- 6) Amplitude of last peak
- 7) Time of last peak
- 8) End of signature status/vehicle presence status

Time values have a range of 12 bits, with the LSB equivalent to 4 msec.

Amplitude values have a range of eight bits and are analyzed only in ratios such that the scaling is not required for classification. Storage is allocated for 16 detectors (8 x 16 = 128 words).

5.4.8.2 Data Output Data Base--This data base consists of:

- BUSWD - A 16-bit word, with each bit representing the presence of a bus on the detector corresponding to that bit position in the 16-bit word.
- VPREC - A 16-bit word, with each bit representing the presence of a vehicle on the detector corresponding to that bit position in the 16-bit word.
- CTR - A counter for each detector showing lengthening of the set time of a given bit in the BUSWD. Count down is (to zero) on each interrupt to control the re-setting of the particular BUSWD bit.

5.4.8.3 Vehicle Classifier Data Base--This data base consists of:

- DCTR - A counter to control sequencing through signature data; counts once for each detectors signature.
- VCVC - Vehicle counters; an array 16 words long that is used in detector failure monitoring. Each word is incremented when the corresponding vehicle detector records a vehicle signature.

5.4.8.4 VCDB--This is an array 20 words long. The following is copied from the signature data block (VCSDB):

- VCDB(1) - Total duration of signature (x 4 msec)
- VCDB(2) - First peak amplitude
- VCDB(3) - Time from "turn on" to first peak (x 4 msec)

VCDB(4) - Second peak amplitude  
VCDB(5) - Time from "turn on" to second peak (x 4 msec)  
VCDB(6) - Last peak amplitude  
VCDB(7) - Time from "turn on" to last peak (x 4 msec)

Note: End of signature status not copied.

The following is determined during the moving/stopped test:

VCDB(8) -  $(VCDB(1) + (VCDB(3) - (VCDB(7)))$

The following is determined during the stopped vehicle classifier:

VCDB(9) -  $(G1 \text{ coefficient for H1 function}) * (VCDB(4))$   
VCDB(10)-  $(G2 \text{ coefficient for H1 function}) * (VCDB(6))$   
VCDB(11)-  $(G1 \text{ coefficient for H2 function}) * (VCDB(4))$   
VCDB(12)-  $(G2 \text{ coefficient for H2 function}) * (VCDB(6))$   
VCDB(13)- H1 function  
VCDB(14)- H2 function

The following is determined in the moving vehicle classifier:

VCDB(15)-  $(G1 \text{ coefficient for K4/K5 function}) * (VCDB(4))$   
VCDB(16)-  $(G2 \text{ coefficient for K4/K5 function}) * (VCDB(6))$   
VCDB(17)-  $(VCDB(16) - (VCDB(17)/(VCDB(2)))$   
VCDB(18)-  $(F1 \text{ coefficient for K4/K5 function}) * (VCDB(5) - (VCDB(3))$   
VCDB(19)-  $(F2 \text{ coefficient for K4/K5 function}) * (VCDB(7) - (VCDB(5))$

VCDB(20) - (VCDB(19) - (VCDB(18)/(VCDB(8))))  
 VCDB(21) - K4 function  
 VCDB(22) - K5 function  
 VCDB(23-25) - Not used

5.4.8.4.1 VCLOG (Vehicle Classifier Vehicle Log)--

VCLOG(1) - Number of signatures rejected as noise (total duration less than 128 msec).  
 VCLOG(2) - Number of signatures that failed gross features test and are thus classified as non-busses (fewer than three peaks).  
 VCLOG(3) - Number of signatures classified by stopped vehicle classifier.  
 VCLOG(4) - Number of signatures classified by moving vehicle classifier.  
 VCLOG(5) - Number of signatures that passed gross features test and were classified as non-busses.  
 VCLOG(6) - Number of signatures classified by busses.  
 VCLOG(7-15) - Not used.

5.4.8.4.2 CLASS--Temporary save location for classification made by VCLAS; used in DMON.

5.4.8.4.3 VPRSNT--Used by VCLAS to transmit to DMON information showing a vehicle is on the detector (=1), or no vehicle is present on the detector (=0). DMON knows with which detector to associate this information (using DCTR).

5.4.8.5 Executive Data Base--EBUF contains the data explained in this subsection:

- ERTCF--Real-time computation sequence compute flag (=1 RTC sequence in process; =0 RTC sequence completed). Each of the save areas below contains the computational environment as stored at that event. The data appear in the following sequence in ESAV, CSAV, and EDSAV:
  - AC0, AC1, AC2, AC3
  - RALU flags
  - CPU stack contents
  - Select flag state

ISV contains only the accumulators and the stack.

- EXAV--Save area for real time clock interrupts.
- CSAV--Save area for COTF operation.
- ISV--Stack-full save area.
- EDSAV--Disconnect save area.
- CTST--Optional uses during software development.
- SSAD--Start address for RAM test.
- SEAD--End address for RAM test.

5.4.8.6 Error Buffers--The buffers for error data are identified as PERR and EERR. These buffers are headed by an error flag word. The bits in the error flag word are assigned individually to error conditions. For each error condition, there are two full words in the error buffer: the first word is the counter for the number of times this error has occurred, and the second word is the error value related to the error condition.

5.4.8.6.1 PERR--VC LAS error flags, counters, and data.

5.4.8.6.2 PERRF--Error flags:

- Bit 0 - Arithmetic overflow in VC LAS.
- Bit 1 - Detector index out of range in VC LAS.
- Bit 2 - Amplitude datum out of range.
- Bit 3 - Time datum out of range.
- Bit 4 - Data out of sequence.
- Bit 5 - Noise.
- Bit 6 - New signature started during classification data copy operation.
- Bit 7 - Signature lost during copy operation.
- Bit 8 - Detector index out of range in PREQ.
- Bit 9 - Preempt request started for downstream detector.



#### 5.4.9 Top Page

While this PROM area is primarily used to control restart initialization, by the JMP 0 instruction at location FFFE HEX, there are other constants for use by the CCU.

#### 5.4.10 Program Listings

The assembled program listing for the Passive Bus Detector Production Prototype Unit is found in Appendix D.

## SECTION 6

### FIELD EVALUATION RESULTS

The stated purpose of the field evaluation in Task F is two-fold:

- 1) Determine the performance of the classifier (accuracy and false alarms).
- 2) Determine the performance of the inductive-loop detector as a vehicle detector.

However, the third, but unstated, purpose was to determine whether or not the classifier performance had been detrimentally affected by reconfiguring the PBD system concept. The reader will recall that the system concept evaluated in Option I of this contract included a fixed-time traffic controller integrated with the classifier. The current concept of the PBD system is a stand-alone classifier which can be used with a variety of existing, or future, traffic controllers.

Although data were gathered regarding the preemption of the Type-190 controller, an evaluation of the benefits of bus priority was not among the test objectives.

#### 6.1 INSTALLATION

The test site chosen for the field evaluation was one of the same sites chosen under Option I: 33rd Avenue and Johnson Street N. E., Minneapolis. This site was selected for the second time to minimize the cost of the test program.

The four existing loop-detector transducers from Option I were again used for this evaluation. Figure 25 is a drawing of the intersection. The loops are installed as an upstream/downstream detector pair on the northbound and southbound approaches to the intersection. A bus classification at the upstream detector initiates the preempt modification of the timing plan to favor the bus by borrowing time from the 33rd Avenue green time. A subsequent bus classification at the downstream detector results in termination of the preempt.

The controller cabinet containing the PBD system and ancillary control equipment was placed adjacent to the existing city controller. The PBD cabinet was wired so that it had continuous control of the intersection.

The signalization on both two-way streets is controlled by red, yellow, and green lights. Pedestrian movements are controlled by WALK and DON'T WALK signals. There are no special bus signal heads and no turning movement signals.

The width of Johnson Street is 40 ft (12.2 m) south of the intersection and 44 ft (13.4 m) north of the intersection. On the northbound approach, a car was parked at the end of the parking zone near the downstream detector to prevent the bus from missing the detector on the curbside. On the southbound approach, however, the bus may miss the downstream detector when pulling over for passenger loading. Consequently, this affected the number of bus signatures processed for each detector during the test sessions.

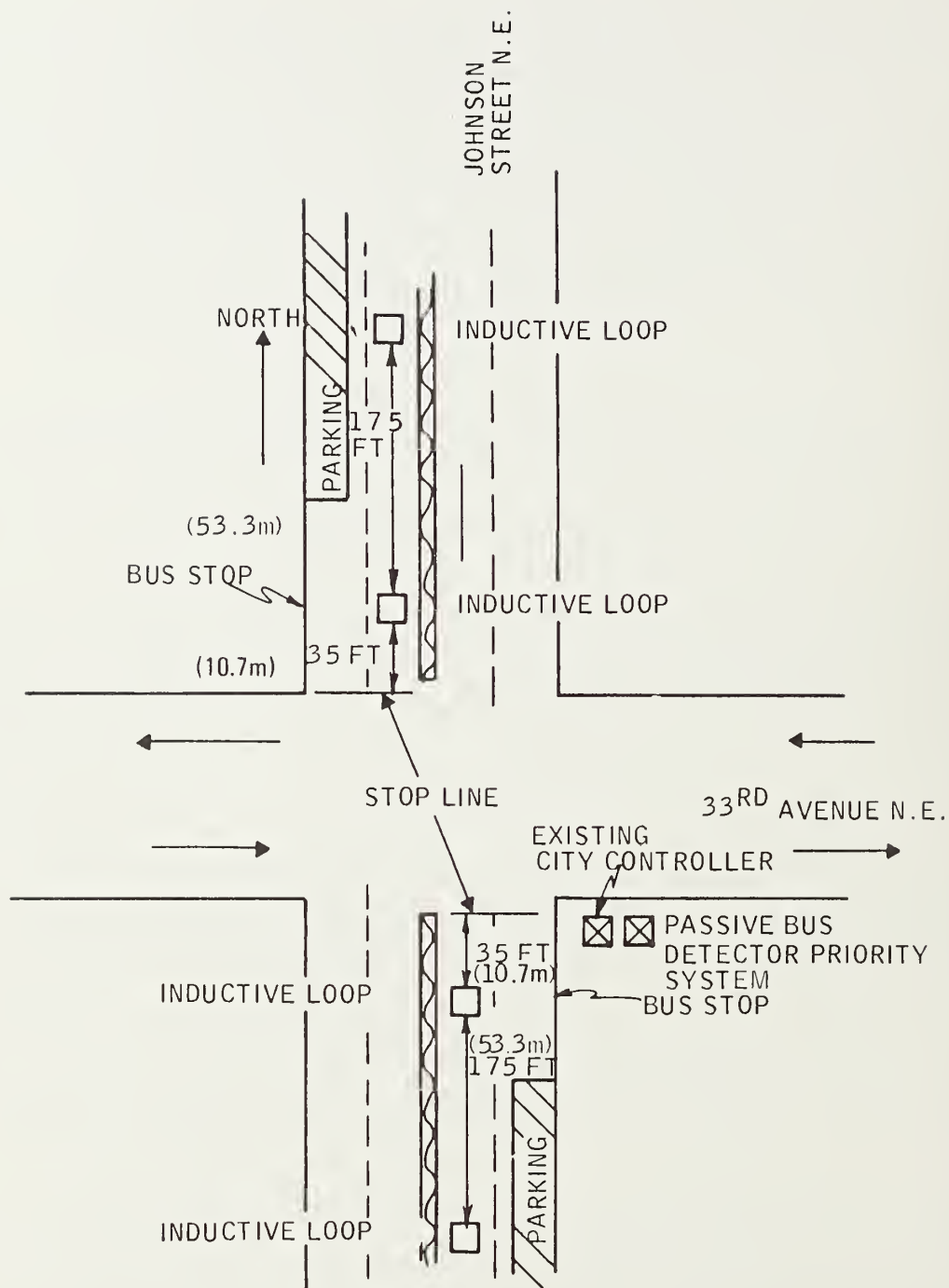


Figure 25. Installation and Demonstration Site, Minneapolis - 33rd Avenue and Johnson St. N.E.

## 6.2 EQUIPMENT DESCRIPTION

The major components of the PBD cabinet were:

- Type-190 Controller
- TMC-1000 Coordinator
- Logic Unit
- Bus Classifier Unit
- Inductive-Loop Detector Unit

Figure 26 shows these units in their respective positions in the cabinet. The operation of these devices, except the Logic Unit, has been covered elsewhere.

The Logic Unit provided the interface between the PBD relay outputs and the Hold and Force OFF inputs on the 190. A simple device, it consisted of a:

- Minimum travel time timer
- Maximum travel time timer
- Maximum extension time timer for each of the dials

The minimum time timer prevented an early termination of preempt due to a formerly parked bus pulling away from the curb after a preempt initiation by a new upstream bus. The maximum travel time timer prevented a maximum extension being given for busses missing the downstream detector. The maximum extension timer took care of multiple busses approaching the intersection at once.

Figure 27 is the schematic diagram of the Logic Unit. Extensions of the Johnson Street (ø2) green time were accomplished by feeding the ø2 Hold

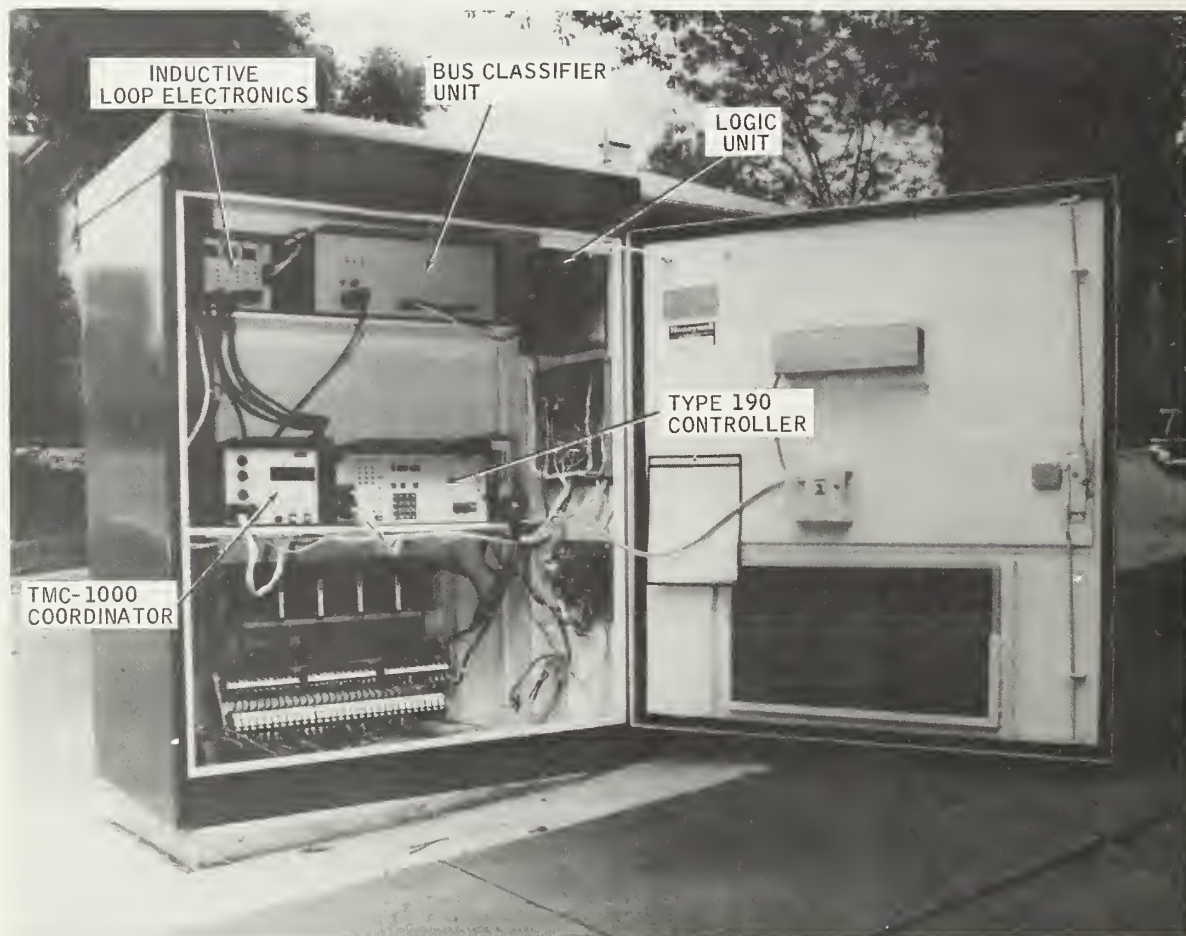


Figure 26. Intersection Cabinet





signal input on the 190. Shortening of the 33rd Avenue (ø4) green was accomplished with the ø4 Omit signal.

The two PBD upstream detector bus call outputs were tied together (OR'ed) to initiate the preempt sequence. The downstream bus call outputs were also OR'ed together to terminate the sequence.

### 6.3 TEST PROCEDURE AND RESULTS

For the PBD 33J tests, three observers were present during the data recording sessions. One observer was near each of the two upstream detectors to determine whether or not the bus traversed the detector within the detection zone for classification. The third observer was positioned at the open controller cabinet to determine the classification result for each bus and for special vehicles.

The time of arrival was noted on a strip-chart recorder for subsequent data reduction. Other information displayed on the strip chart were 1-second time marks, bus classification output from each sensor channel, and the main street green light duration.

#### 6.3.1 Bus Detector/Vehicle Classifier Performance

The vehicle classifier algorithm is designed to discriminate between the standard urban transit busses manufactured by General Motors, Flxible, American Motors General, and all other vehicles. Therefore, the performance of the bus detector hardware and the vehicle classifier software was measured in terms of successful bus classifications and the number of false bus classifications for non-bus vehicles. Only the AMG and Flxible busses were running this route during this test period.

The design goal of this passive vehicle classification technology is to properly discriminate all preempt buses which pass over the detector transducer within  $\pm 4$  ft ( $\pm 1.2$  m) of the centerline of the 6 x 6-foot (1.8 x 1.8-m) inductive loop. Busses which crossed the detector outside of this detector zone were not required to be properly classified.

During the test sessions, most of the busses passed within the detection zone of the upstream detector on each approach. At the downstream detectors, however, some busses missed the detection zone due to moving to the curb for passenger loading. For the downstream detector on the northbound approach, a parked car could preclude the passage of the bus on the curbside of the detection zone. During most but not all of the test sessions, a parked car was in such a position. Consequently, the total number of bus signatures at this downstream detector is somewhat lower than the upstream detector.

On the southbound approach, however, a longer "no parking" zone is provided for the passenger loading zone, and a bus which stops for passengers may miss the detection zone on the curbside of the loop detector. Consequently, the total number of busses at the downstream detector was approximately half of the number of busses passing over the upstream detector on the southbound approach.

The overall bus classification performance is summarized for each of the four detectors in Table 1. Three of the four detectors exceed the performance goal of 95 percent correct classification of busses. Detector 3 achieved only 93.75 percent correct classifications. The overall figure for the four detectors is 95.57 percent of the total of 271 bus signatures. All data were recorded without any adjustment to the vehicle classifier.

TABLE 1. BUS DETECTOR/VEHICLE CLASSIFIER PERFORMANCE

Detector No.	Direction	Bus Classification	Busses	Percent
1	Northbound upstream	78	80	97.5
2	Northbound downstream	76	80	95
3	Southbound upstream	75	80	93.75
4	Southbound downstream	30	31	96.774
Total		259	271	95.57

The misclassifications of busses are summarized in Table 2 in terms of bus manufacturer and whether or not the bus had stopped over the detector. Note that 41.6 percent of all misclassifications occurred at detector 3, and 33.3 percent at detector 2. Three-fourths of the misses were Flexible busses, while the remaining fourth were AMG busses. Moving busses accounted for 83.3 percent of the misses.

Due to program schedule limitations, the margin of classifier error for these misses was not seriously studied. However, with the help of the FORTRAN classifier program and signatures collected on-site, performance improvements could be accomplished.

Since the downstream detector is placed at one bus length from the stop bar, the bus can uncover part of the loop if it stops beyond the stop bar. Noise or interference from a trailing vehicle may distort the bus signature at the trailing edge and result in misclassification.



TABLE 2. MISCLASSIFICATION OF BUSES

Detector No.	Direction	Bus Type	
		Flxible	AMG
1	Northbound upstream	(M) 2 (S) 0	
2	Northbound downstream	(M) 2* (S) 2*	
3	Southbound upstream	(M) 2 (S) 0	(M) 3 (S) 0
4	Southbound downstream	(M) 1 (S) 0	
Total		9	3

Overall 12 misses: 10 moving bus signatures (M)  
2 stopped bus signatures (S)

\* Faulty detection loop, see subsequent paragraphs.

Performance of the PBD system as a vehicle detector was indirectly evaluated in two separate locations. During the preliminary tests at Honeywell's Vehicle Test Facility, the following procedure was performed. After the sensitivity for bus classification was adjusted, a bus and three other passenger cars were run directly over the loop. In all cases, vehicle detection was observed. These vehicles were then run alongside, just outside, the loop to determine what adjacent lane effects might occur, if any. In all cases, no adjacent lane detections occurred until the vehicle, once again, partially covered the loop.

At the intersection test site, 33rd and Johnson, the operation of vehicle detection was only casually observed due to the heavy workload of the observers during the data collection periods. However, no unusual vehicle detection operation was ever observed. In fact, no constant vehicle calls

were ever noted due to long-term drift of the loop.\* This is not surprising, since the preprocessor in the BCU is constantly compensating for the drift of each and every loop.

### 6.3.2 False Bus Classifications

One false bus classification was observed during the test period and this was an International Carry-All-type vehicle pulling a low-bottom, hard-top camping trailer and an inverted aluminum rowboat on top of the trailer. Only one false alarm occurred out of 271 bus signatures and an unrecorded number of vehicle signatures processed.

### 6.3.3 Bus Preempt Operation

For the busses which were countable over the upstream detectors 1 and 3, 48.1 percent were granted a preempt of the timing plan. In several cases, other busses derived benefit from a preempt already in progress from another bus which arrived earlier in the same cycle of the timing plan. There was no failure of the timing algorithm to perform as designed.

Preempts were initiated every time a bus classification was made on an upstream detector but many were cleared out when a downstream classification was made within the timing constraints of the logic module. Only those which resulted in an actual modification of the cycle composition are referred to in the above 48.1 percent.

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\* The one exception is the failed loop which caused the amplifier to saturate, rendering that channel completely inoperative.



#### 6.3.4 Travel Time Saved

Travel time saved by preempts (ref. Table 3) is defined in the following manner:

- Force off causes an early return to  $\phi 2$  green. This is the amount of time entered in the tabulation.
- Extension time is that time which would have elapsed during the main-street red portion of the cycle time. (This time was different for each test.)

TABLE 3. TRAVEL TIME SAVED BY PREEMPT

##### A. Travel Time Saved via Force Off's

Parameter	9/19/77	9/26/77	10/13/77	Total
Total time saved (sec)	289.5	308	625.5	1232
No. of entries	19	18	29	66
Average (sec)	15.237	17.111	21.569	18.667

##### B. Travel Time Saved via Extension

Parameter	9/19/77	9/26/77	10/13/77	Total
Total time saved (sec)	129*	200*!	**	329
No. of entries	3*	5*!	**	8
Average (sec)	43*	40*!	**	41.125

\* Does not include an extension preempt which was concluded by a force off. The logic timers allow an extension preempt to be granted and, if not cleared by the downstream sensor, will also allow a force-off preempt to occur.

! Includes one bus which shared an extension preempt granted to another.

\*\* No extensions granted during the 8-hour test interval.

### 6.3.5 The Field Test

For these tests, a strip-chart recorder was set up along side the controller cabinet to record the main street green signal, bus classification, and a 1-second time trace. A Sonalert was also connected to the classifier test circuit to supply an audible classification signal.

The controller was switched from "Remote" dial to "Free, Dial 2," and Phase 4 was called up and changed to "Maxi Recall" for the test. Phase 4 parameters were recorded before changing and were restored to these at the conclusion of the test for that day. Phase 2 parameters were not recorded and, in retrospect, should have been, since the main street green cycle varied from test to test.

The city has another loop in close proximity to the southbound upstream loop, No. 3, that is used to monitor traffic density. This was turned "OFF" for the test and restored to "ON" at the conclusion of test day. There was some concern that signal excitation of this loop would couple through a passing bus and cause interference; however, there was no evidence that this had occurred.

### 6.3.6 Strip-Chart Recording

The recorder used was a two-channel device with a separate pen for event and timing. The top trace was the main street green interval, and the second trace was a composite of the channel classification signals, with a different amplitude for each channel so that if a coincidence occurred, the two detectors could be determined. The timer trace of 1-second intervals enabled the extraction of preempt duration from the nominal timing cycle.

The recorded main street green signal had the form shown in Figure 28.

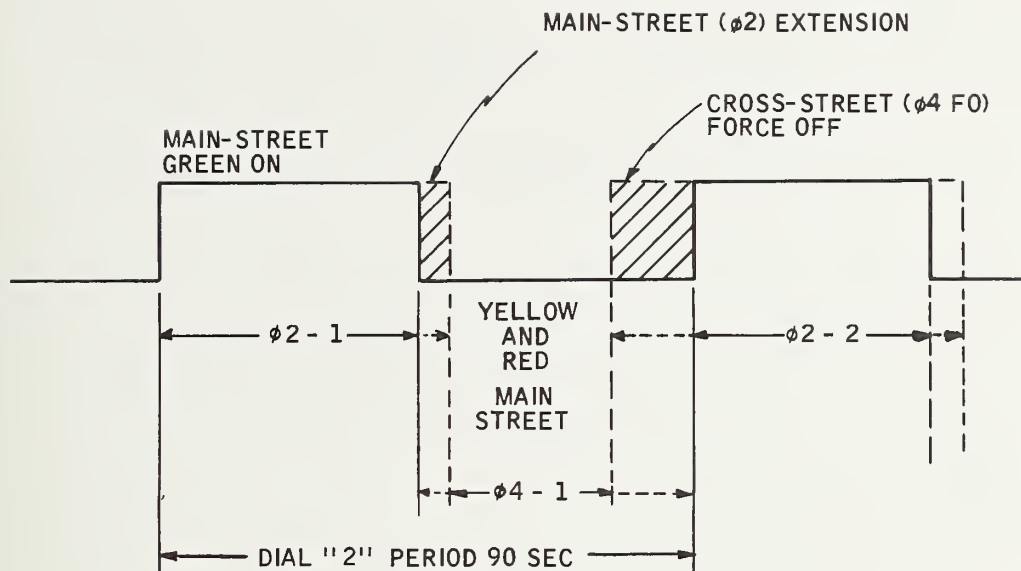


Figure 28. Main Street Green Signal Format

The normal cycle is shown with the solid line with the two shaded (dotted) areas being the extension of Phase 2 green and/or the Phase 4 green force off. The  $\phi 2-1$  symbol is the reference Phase 2 green time which varied from test to test but remained constant except for preempts for the test day. The Phase 2 extension time, then, is the difference between the actual recorded time and the day's reference or nominal time.

The  $\phi 4-1$  symbol indicates the time during which the main street is not green (actually represents the cross-street green and main-street yellow). In the absence of a preempt signal,  $\phi 2-1 + \phi 4-1$  is 90 seconds, so, again, the  $\phi 4$  force-off time is the difference between the nominal 90-second period and recorded Phase 2 green restart (Phase 4 termination). The symbols  $\phi 2-2$  and  $\phi 4-2$  represent the second cycle for those situations where interaction between cycles occur by bus arrival-time variations.

### 6.3.7 Data Reduction

From the strip-chart recording, the following data were tabulated:

- Arrival time of bus where noted
- Bus number where noted
- Direction of travel
- Upstream classification time from reference  $\phi 2-1$  start
- Downstream classification time from  $\phi 2-1$  start
- $\phi 2-1$  termination time
- $\phi 4-1$  termination time
- $\phi 2-2$  termination time
- $\phi 4-2$  termination time
- Cycle interaction from bus arrival times

From the above tabulation, the following determinations were made:

- No.  $\phi 2$  extensions
- No.  $\phi 4$  force offs
- Average  $\phi 2$  extension time
- Average  $\phi 4$  force-off time
- Total number of preempts granted
- Percent of granted to potential preempts
- Misclassification of bus types
- Misclassification of bus signatures stopped/moving
- Detectors versus misclassifications

See Appendix E for tabulated data.

#### 6.3.8 Component Problems and/or Failures

The northbound downstream detector loop No. 2 exhibited frequent need for retuning. This was eventually found to be due to a faulty loop having less than normal resistance and a low resistance to the shield ground. No problems were experienced due to inability to sense and classify a bus during field test days. Day-to-day changes required retuning but never during the field test day itself. After the loop problem was identified, the tuning was checked after each misclassification and determined to be satisfactory.

Other problem areas were:

- Prior to the 8-hour surveillance tests, the ILDU power supply regulator chip ( $\mu$ A723) was found to be intermittent and was replaced.
- At the same time, a thumbwheel switch for the ILDU channel 4 (amplifier 1) was found to have a shorted MSB section. This was replaced also.
- After the first 8-hour surveillance test, the 190 controller failed. No positive cause was ever determined for the questionable operation except that the unit functioned satisfactorily with the coordinator power switch off. This was turned on for the second 8-hour test, and then turned off when concluded. The city later repowered the unit and left it on.



## SECTION 7

### CONCLUSIONS AND RECOMMENDATIONS

#### 7.1 CONCLUSIONS

The 16-channel PBD system developed under this contract in Option II has made it possible to significantly advance the state of the art in traffic control strategy. The successful evaluation of the PBD has shown that a mass-transit bus priority system can be accurate, easy to set up and operate, and be valuable in aiding busses get through intersections with minimum disruption of other traffic. This system should encourage bus ridership by improving the on-time performance on a variety of bus routes. The traffic engineer, by selecting from a variety of traffic controllers to operate with the PBD, can tailor bus priority systems to a variety of situations.

The only potential drawback to the PBD developed under this contract is system cost. The 16-channel requirement of the PBD exceeds the requirement for most installations. This has no direct bearing, however, on the technical concept of passive bus detection as developed herein.

#### 7.2 RECOMMENDATIONS

Although the prototype development program was successful, several recommendations are made for future development work. Specifically, two of these concern the reduction of PBD production costs via a reduction of design and performance goals.

A general feeling exists that a 16-channel BCU, such as this model, is perhaps one of the largest number of channels ever required at one traffic intersection. Furthermore, a general feeling exists that most control



situations would require only two to eight channels. If these reduced requirements could be brought to bear on the PBD design, the BCU could possibly take advantage of newer, less-expensive (and slower) microprocessors. One recommendation, then, is that a tradeoff study be performed between PBD system cost versus number of channels per BCU.

Another factor which has the potential of reducing PBD system cost is allowing the number of false classifications to increase. At the present time, the false classification rate is under 1.0%. If this were allowed to increase, the classification algorithms could be simplified, thus reducing hardware performance and cost. Therefore, the recommendation is made that a realistic false classification rate and its impact on PBD system cost be studied.

Finally, Honeywell has received an inquiry concerning the feasibility of achieving a three-class classifier in this PBD. The desired classes are: cars, trucks, busses. The applications for a three-class system can easily be postulated. One is where a traffic mix is desired for traffic-responsive control. Another is that where vehicle speed is desired, it can be obtained with a one-loop (as opposed to two-loop) device once the vehicle type (i. e., length) is known. Fewer loops mean less maintenance in colder climates. The recommendation is made, then, that the market be surveyed for this need and the feasibility of achieving a multiclass classifier with the PBD be studied.



# APPENDIX A

## COMPENSATION DERIVATIONS

### COMPENSATION CURVES

The compensation curves were developed as follows. The amount of tuning capacitance needed to achieve null was noted for four loop/ lead-in induc-  
tances, at two temperatures (see Table A-1). The test location was an  
asphalt street in Minneapolis.

Table A-1. Percent Capacitance Change

Lead-in Length		Capacitance (farads) at		Percent Change
feet	meters	20° F (-7°C)	40° F (+4°C)	
250	76.0	0.01846	0.01856	0.54
75	20.3	0.01762	0.01774	0.17
301	91.7	0.01646	0.01656	0.68
255	77.7	0.02415	0.02420	0.61

When the percentage changes were normalized to the lead-in length accord-  
ing to

$$k = \frac{\% \text{ change}}{^{\circ}\text{F} \times \text{length (ft)}} \quad (1)$$

Table A-2 was derived.

Table A-2. Constants

Lead-in Length		k
feet	meters	
250	76.0	$5.4 \times 10^{-5}$
75	20.3	$5.67 \times 10^{-5}$
301	91.7	$5.65 \times 10^{-5}$
255	77.7	$5.98 \times 10^{-5}$

The average constant, k, value is  $5.675 \times 10^{-5} \% / ^\circ\text{F ft.}$

These steps imply that the amount of compensation is proportional to the total total tuning capacitance:

$$C \text{ backoff} = \% \text{ change } C \text{ total or} \quad (2)$$

$$C \text{ backoff} = ^\circ\text{F} \times \text{ft } C \times k \times \frac{Q^2}{W_0^2 L (1 + Q^2)} \quad (3)$$

Notice that Equation (3) involves the value of Q.

We have measured three Q values at the following lead-in lengths (operating frequency,  $f_o = 100 \text{ KHz}$ , Belden 8718):

50 ft. (15.2m)	$Q = 16$
250 ft. (76.0m)	$Q = 7.7$ and
350 ft. (106.4m)	$Q = 6.7$

To get Q values at intermediate lengths of 100 feet (30.4m) and 150 feet (45.6m), the above values were subjected to a least-squares fit to the quadratic equation

$$Q = ax^2 = b x + c \quad (4)$$

where x = lead-in length in feet.

The coefficients with less than 0.004 percent error are:

$$a = 0.1117 \times 10^{-3}$$

$$b = 0.7600 \times 10^{-1}$$

$$c = 0.1997 \times 10^2$$

and yield Q values of

$$100 \text{ ft (30.4m)} \quad Q = 13.1$$

$$150 \text{ ft (45.6m)} \quad Q = 10.8$$

The above information was inserted in Equation (3) using a time-share computer program in BASIC (see below). The capacitance backoff was normalized to 150°F (65°C) and resolved into an amount of thumbwheel setting change. Since it was apparent that the lead-in length is a primary Q-determining factor, the same Q quadratic coefficients were used for the reinforced roadway situation. However, this assumption was not investigated.

# TIME-SHARE COMPUTER PROGRAM "BASIC"

## LIST ROG

```
01 D = 50
03 Q = 16
05 F = 100E + 03
07 K4 = 5.68E - 05
09 K3 = .001
11 L1 = 72E - 06
13 KI = 24E - 12
15 K2 = 2.2E - 07
17 T0 = 150
19 T1 = 150
21 PRINT, 23
23 FMT, X9, "C BACKOFF", X9, "TEMP", X9, "TOTAL C"
25 W = 6.28*F
27 L = L1 + K2*D
29 C = Q*/(W*W*L*(1 + Q*Q)
31 P = (T1 - T0)*D*K*4*C/100
33 PRINT, 35B, T1, C
35 FMT, X5, F4, X7, 15, X5, E4, 4
37 IF T1 = -30, THEN 43
39 T1 = T1 - 30
41 GO TO 31
43 END
```



where

D = Loop lead-in length (ft)

Q = Quality factor of circuit

F = Operating frequency (Hz)

K4 = Constant (Eq. 1)

L1 = 6-ft x 6-ft three-turn loop (heneries

K1 = Lead-in capacitance per foot (Belden) (farads)

K2 = Lead-in inductance per foot (heneries)

T0 = Temperature ( $^{\circ}$ F)



APPENDIX B  
SCHEMATICS, DRAWINGS, AND PARTS LISTS

The following schematics, drawings, and parts lists are contained in this appendix:

<u>Drwg. No.</u>	<u>Subject</u>	<u>Revision</u>
YG1191A01	Detector, Bus	Original
28021592	Cable Assembly, Power - Loop Detector	A
28021595	Cable Assembly, BCU to Loop Detector	A
28021596	Cable, Loop Detector	A
28021597	Cable Assembly, Bus Classifier Unit	A
28021574	Bus Classifier Unit Assembly	A
10059917	Schematic Diagram, Power Supply, Bus Detector	B
28021575	Chassis	A
28021576	Rack, Card	A
28021577	Cover Assembly	A
28021578	Bracket, Thermostat	Original
28021579	Harness Assembly, Power Supply	A
28021580	Silkscreen, Chassis	Original
10063318	Printed-Circuit Assembly Motherboard, BCU	A
10063319 (4 sheets)	Printed-Circuit Board Motherboard, BCU	Original

<u>Drwg. No.</u>	<u>Subject</u>	<u>Revision</u>
Signal List - BCU Backplane (6 sheets)	Motherboard Interconnect List	Original
10059900	Schematic Diagram, PROM Memory, Bus Detector	C
10059900	Parts List, Bus Detector, PROM Memory	C
10059900	Printed-Circuit Assembly, PROM Memory BCU	Original
10063320 (4 sheets)	Printed-Circuit Board - PROM Memory, BCU	Original
10059899	Schematic Diagram, I/O Card, Bus Detector	G
10059899 (sheet 1)	Parts List, Bus Detector, I/O	A
10059899 (sheet 2)	Parts List, Bus Detector, I/O	D
10059899	Printed-Circuit Assembly, I/O, BCU	Original
10063321 (5 sheets)	Printed-Circuit Board-I/O	Original
10059904 (2 sheets)	Schematic Diagram, Preprocessor Control Decoding Card No. 1, Bus Detector	E
10059904 (sheet 1)	Parts List, Preprocessor Control Decoding Card No. 1	B
10059904 (sheet 2)	Parts List, Preprocessor Control Decoding Card No. 1	D
10059904	Printed-Circuit Assembly, Preprocessor No. 1, BCU	Original
10059901 (sheet 1)	Schematic Diagram, Cycle Steal Control/ Address, Preprocessor Card No. 2, Bus Detector	E

<u>Drwg. No.</u>	<u>Subject</u>	<u>Revision</u>
10059901 (sheet 2)	Schematic Diagram, Cycle Steal Control/ Address, Preprocessor Card No. 2, Bus Detector	D
10059901	Parts List, Cycle Steal Control/Address, Preprocessor Card No. 2	C
10059901	Printed-Circuit Assembly, Preprocessor No. 2, BCU	Original
10063322 (5 sheets)	Printed-Circuit Board, Preprocessor No. 1, BCU	Original
10063323 (5 sheets)	Printed-Circuit Board, Preprocessor No. 2	Original
28021581	Loop Detector Assembly	A
28021582	Chassis, Bottom	A
28021583	Chassis, Top	A
28021584	Bracket	Original
28021585	Bracket, Shield	Original
28021586	Cover, Rear	Original
28021587	Panel, Front	Original
28021588	Cover, Top	Original
28021589	Cable Assembly, Power Supply	Original
28021590	Cable Assembly, Signal	A
28021591	Silkscreen, Front Panel	Original
28021593	Panel, Front	A
28021594	Silkscreen, Detector Mod	A

<u>Drwg. No.</u>	<u>Subject</u>	<u>Revision</u>
10059923	Interconnecting Diagram, Loop Electronics, Bus Detector	C
10059902	Schematic Diagram, Power Supply, Loop Electronics, Bus Detector	D
10059902	Parts List, Power Supply, Loop Electronics	D
10059902	Printed-Circuit Assembly, Relay and Power Supply, Loop Electronics	Original
10063315 (5 sheets)	Printed-Circuit Board - Relay and Power Supply	Original
10059903	Schematic Diagram, Loop Electronics, Bus Detector	D
10059903 (sheet 1)	Loop Electronics	B
10059903 (sheet 2)	Loop Electronics	A
10059903 (sheet 3)	Loop Electronics	B
10059903	Printed-Circuit Assembly, Loop Electronics	Original
10063310 (5 sheets)	Printed-Circuit Board - Loop Electronics	Original
10063324 (4 sheets)	Printed-Circuit Board - Thumbwheel	Original
10063313	Printed-Circuit Assembly Motherboard, Loop Electronics	A
10063314 (4 sheets)	Printed-Circuit Board - Loop Electronics Motherboard	Original



<u>Drwg. No.</u>	<u>Subject</u>	<u>Revision</u>
10063311	Printed-Circuit Assembly, Extender Loop Electronics	Original
10063312 (4 sheets)	Printed-Circuit Board - Extender	Original



5 4 3 2 1

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM

HONEYWELL PART NO.
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REVISIONS			DATE	APPROVED
ZONE	LTR	DESCRIPTION		

THIS SYSTEM CONSISTS OF THE FOLLOWING:

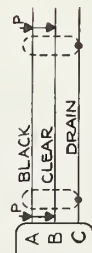
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|----------------------------------|----------|
| BUS CLASSIFIER UNIT ASSY         | 28021574 |
| LOOP DETECTOR ASSY               | 28021581 |
| CABLE ASSY, POWER-LOOP DETECTOR  | 28021592 |
| CABLE ASSY, BCU TO LOOP DETECTOR | 28021595 |
| CABLE, LOOP DETECTOR             | 28021596 |
| CABLE ASSY, BUS CLASSIFIER UNIT  | 28021597 |

TOLERANCES UNLESS NOTED OTHERWISE X ± .XX ± .XXX ±		90° FORMED ANGLES ±.1 .1 ±.1	DRAFTSMAN CHECK DEV ENGR PROJ ENGR RELIABILITY	11/7373 HONEYWELL INC. AEROSPACE AND DEFENSE GROUP AERO ST PETERSBURG 480 MONTGOMERY AVE DETROIT MI 48201
FINISH-NOTE MATL		CONTRACT NO.	DETECTOR, BUS	
NEXT ASSY USED ON APPLICATION		SIZE B27327	CODE IDENT NO. YG1191A01	DRAWING NO. YG1191A01
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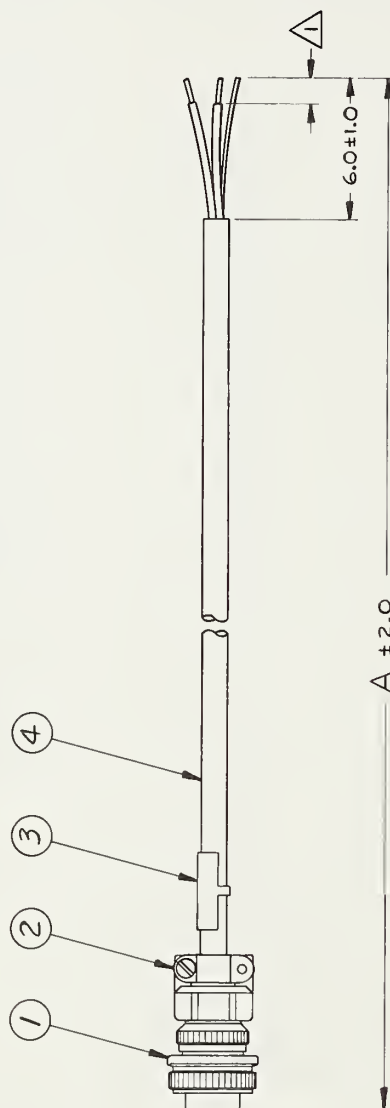




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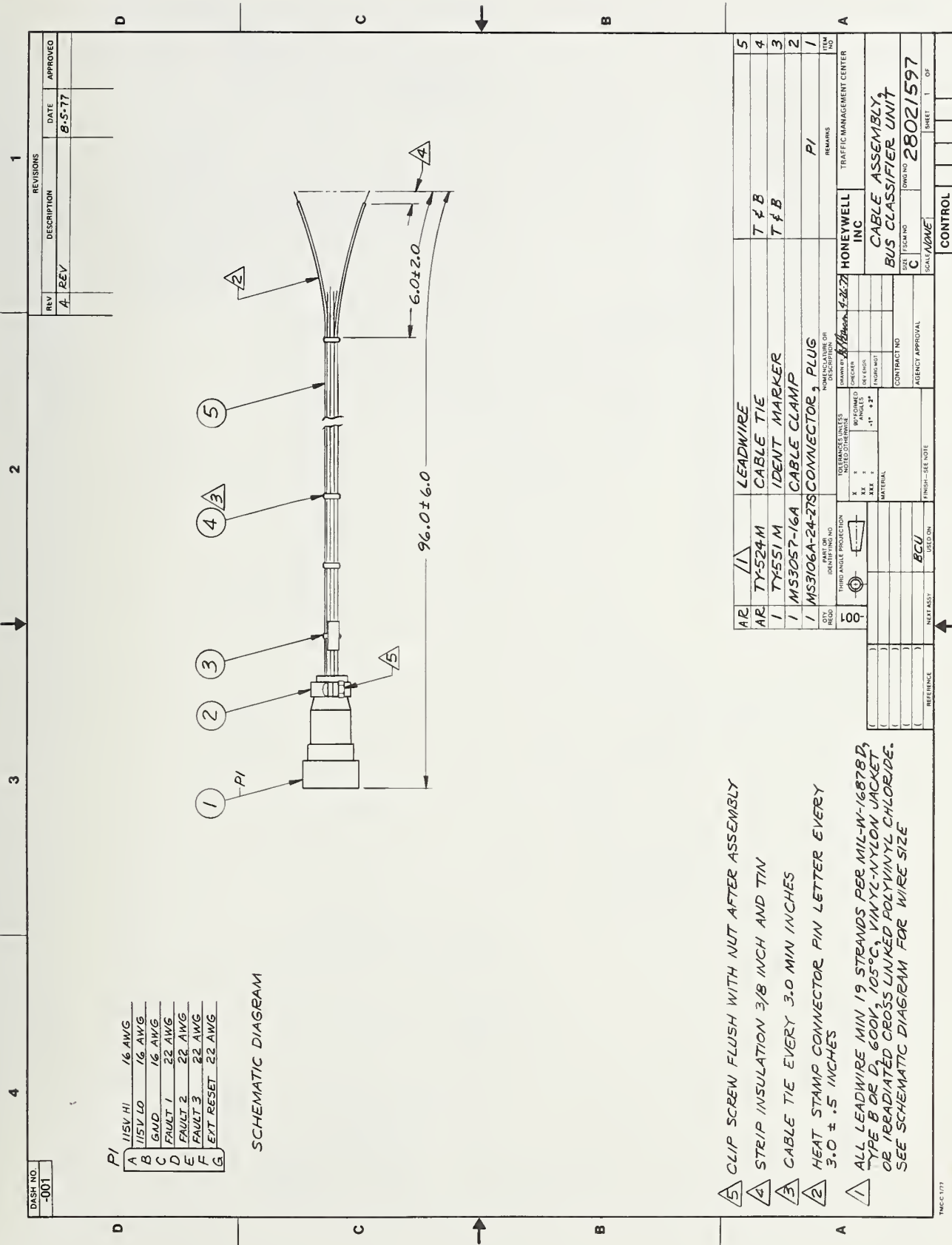
## SCHEMATIC DIAGRAM

[illegible]

2 - BAG AS ASSY AND MARK WITH PART NO.

1- STRIP INSULATION  $\frac{3}{8}$  INCH AND TIN





PI	115V HI	16 AWG
A	115V LO	16 AWG
B	GND	16 AWG
C	FAULT 1	22 AWG
D	FAULT 2	22 AWG
E	FAULT 3	22 AWG
F	EXT RESET	22 AWG
G		

SCHEMATIC DIAGRAM

- 5 CLIP SCREW FLUSH WITH NUT AFTER ASSEMBLY
- 4 STRIP INSULATION 3/8 INCH AND TIN
- 3 CABLE TIE EVERY 3.0 MIN INCHES
- 2 HEAT STAMP CONNECTOR PIN LETTER EVERY 3.0 ± .5 INCHES
- 1 ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878D, TYPE B OR D, 600V, 105°C, VINYL-NYLON JACKET, OR IRADIATED CROSS LINKED POLYVINYL CHLORIDE. SEE SCHEMATIC DIAGRAM FOR WIRE SIZE

REV	DESCRIPTION	DATE	APPROVED
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AR	11	LEADWIRE	5
AR	TY-524M	CABLE TIE	4
I	TY-551M	IDENT MARKER	3
I	MS3057-16A	CABLE CLAMP	2
I	MS3106A-24-27S	CONNECTOR, PLUG	1

QTY	REQD	PART OR IDENTIFYING NO	DESCRIPTION	REMARKS	ITEM NO
50			HEAT STAMP CONNECTOR, PLUG	PI	1

DESIGNED BY	4-26-74	HONEYWELL INC	TRAFFIC MANAGEMENT CENTER
CHECKED BY			
APPROVED BY			
CAD			
CONTRACT NO			
AGENCY APPROVAL			
SCALE	AS SHOWN		
DWG NO	28021597		

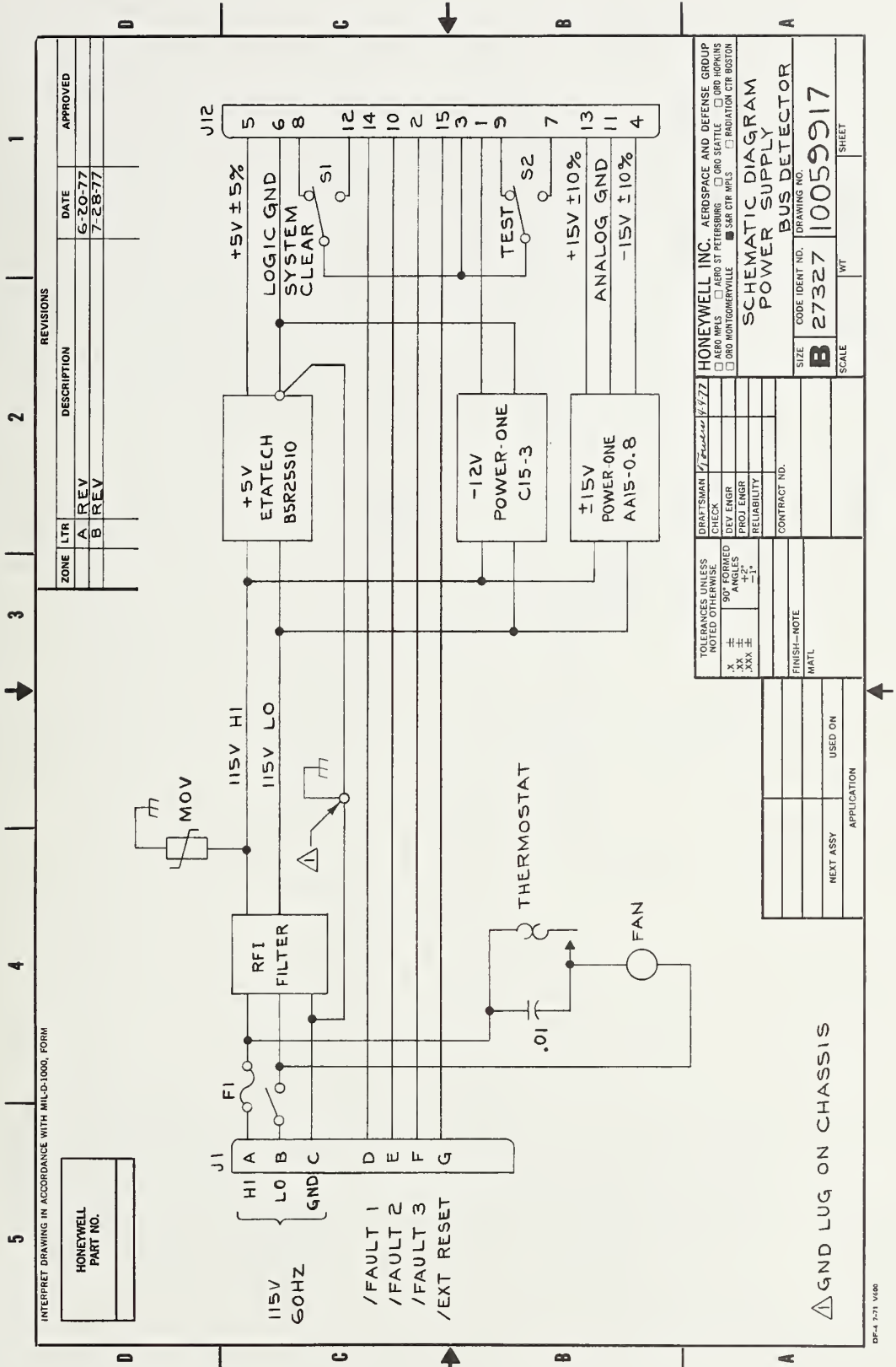
  

REFERENCE	NEAT ASST	USED ON	FINISH - SEE NOTE

CONTROL	SHEET	1	OF
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REVISIONS			DATE	APPROVED
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B	REV		7-28-77	

HONEYWELL PART NO.	

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TOLERANCES UNLESS NOTED OTHERWISE: X ± .01 XX ± .005 XXX ± .0025		CONTRACT NO. FINISH-NOTE MATL	
DRAFTSMAN J. J. J. 4/77 CHECKED DESIGNED PROL. ENGR RELIABILITY		APPLICATION NEXT ASSY USED ON	





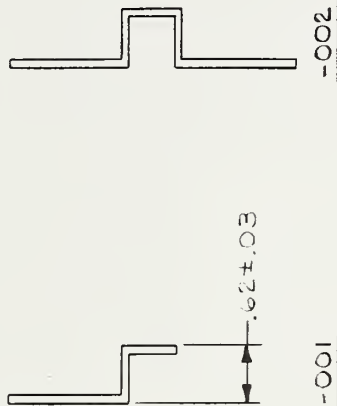
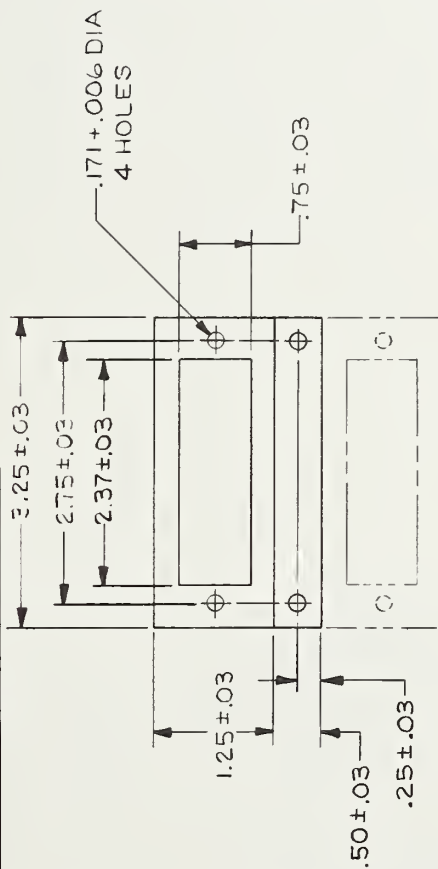






PART NO.	CONFIG.
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-002	2 THERMOSTATS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1001

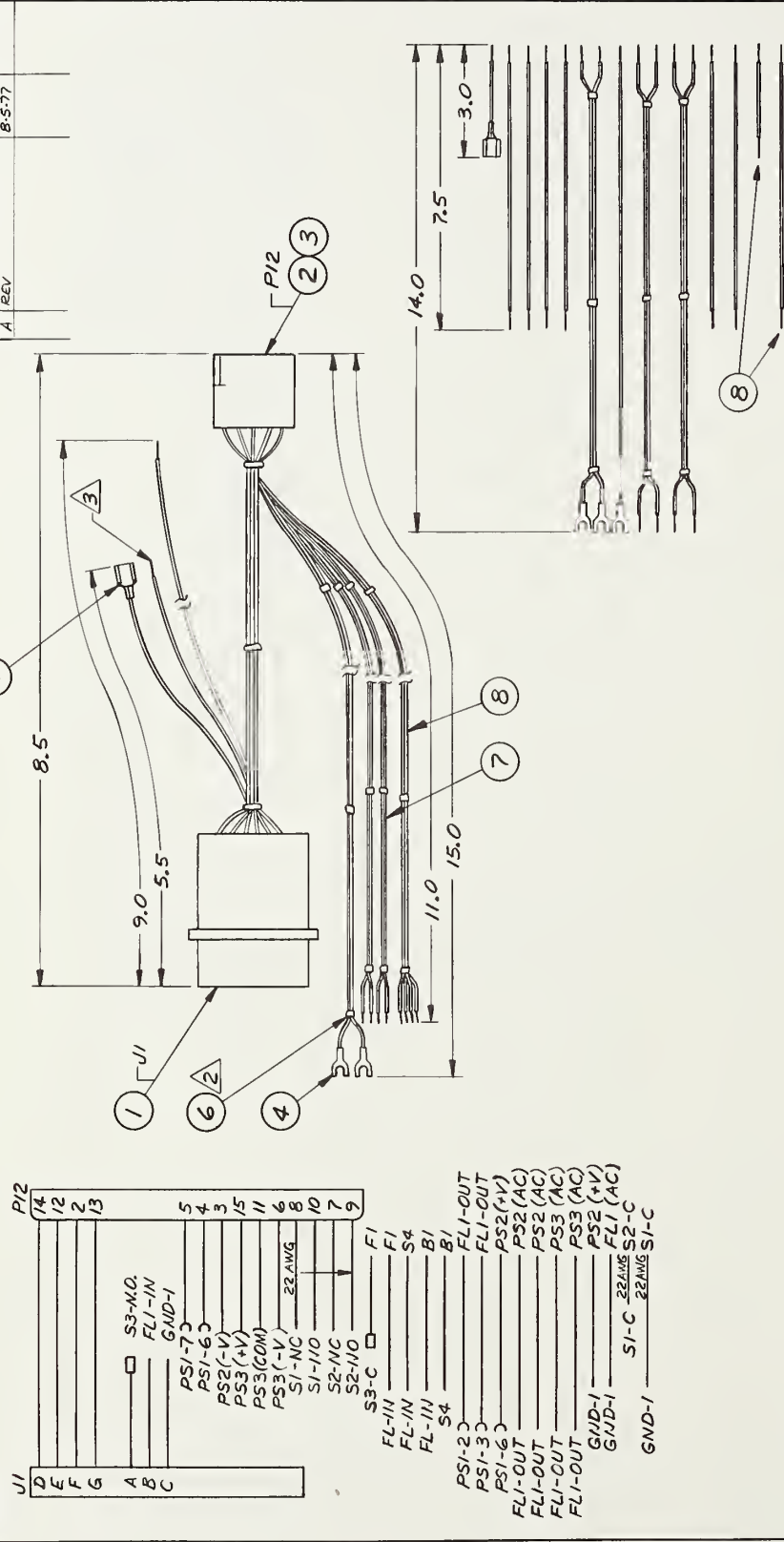
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QAP 8 10/71

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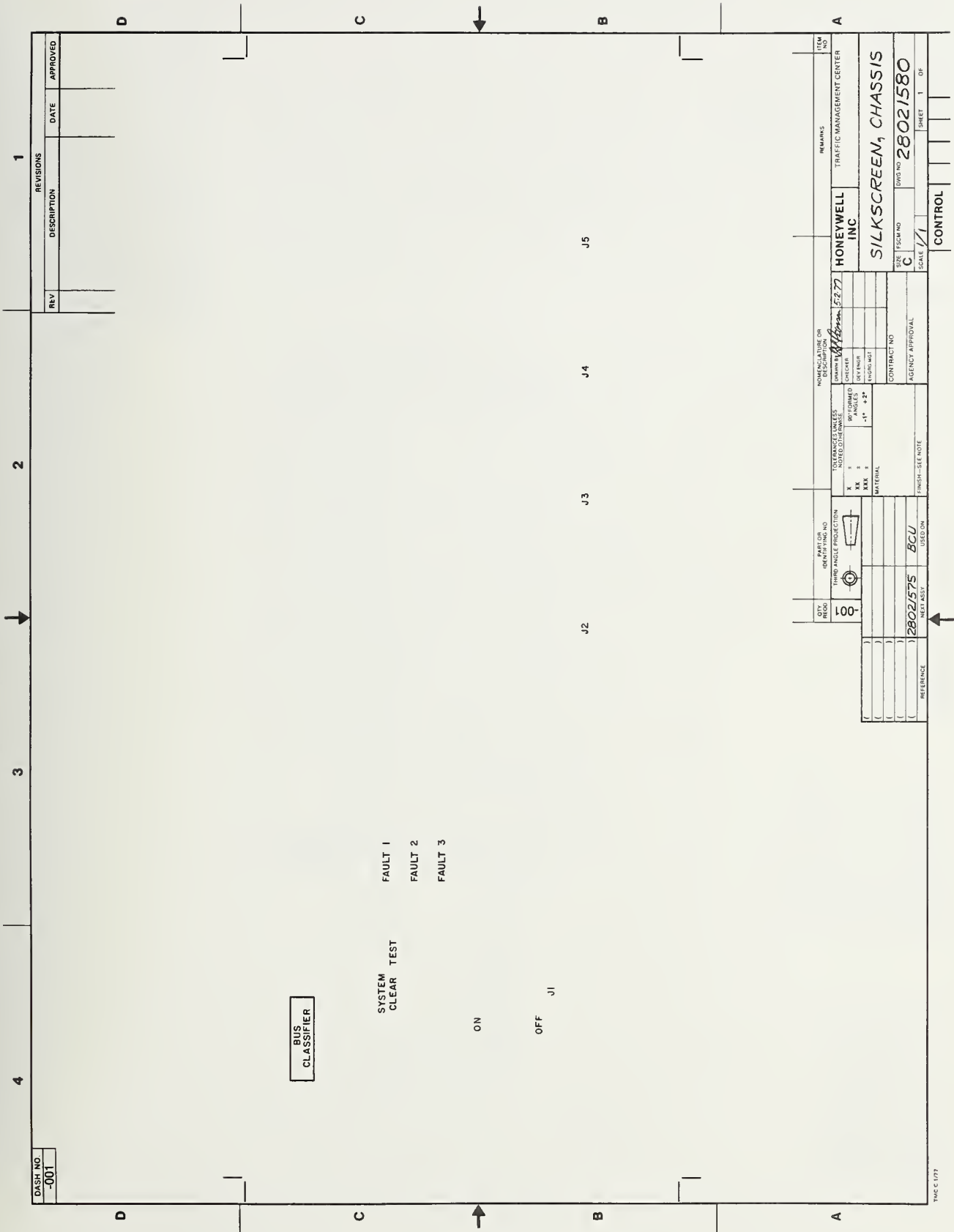
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3	C
15	
11	
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FI	
FI	
S4	
BI	
BI	
PSI-2C	
FLI-OUT	
PSI-3C	
FLI-OUT	
PSI-6C	
PS2(+V)	
FLI-OUT	
PS2(AC)	
FLI-OUT	
PS2(AC)	
FLI-OUT	
PS3(AC)	
FLI-OUT	
GND-I	
PS2(+V)	
FLI(AC)	
GND-I	
SI-C 22AWG S2-C	
22AWG SI-C	

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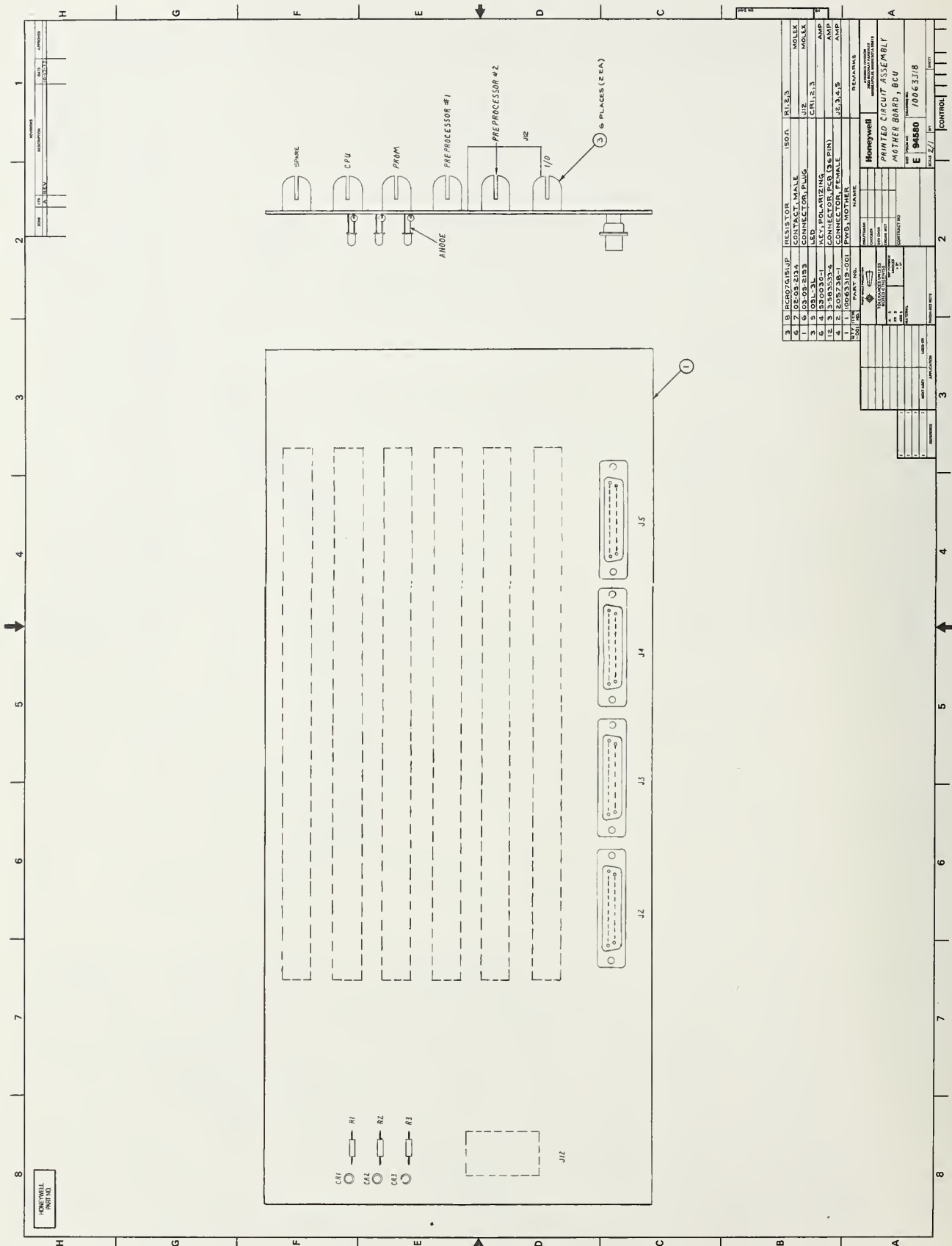
4 - BAG AS ASSEMBLY AND MARK WITH PART NO.  
 3 - STRIP INSULATION 3/8 INCH AND TIN  
 2 - CABLE TIE EVERY 3 INCHES  
 1 - ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878 D,  
 TYPE B OR D, 600V, 105°C, VINYL-NYLON JACKET  
 OR IRRADIATED CROSS LINKED POLYVINYL CHLORIDE



DASH NO.  
-001

REVISIONS		
REV	DESCRIPTION	DATE

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TOLERANCES UNLESS NOTED OTHERWISE		TOLERANCES UNLESS NOTED OTHERWISE		TOLERANCES UNLESS NOTED OTHERWISE		TOLERANCES UNLESS NOTED OTHERWISE	
XX ±		XX ±		XX ±		XX ±	
XXX ±		XXX ±		XXX ±		XXX ±	
-1" ±		-1" ±		-1" ±		-1" ±	
MATERIAL		MATERIAL		MATERIAL		MATERIAL	
CONTRACT NO.		CONTRACT NO.		CONTRACT NO.		CONTRACT NO.	
AGENCY APPROVAL		AGENCY APPROVAL		AGENCY APPROVAL		AGENCY APPROVAL	
28021575		BCU		28021580		28021580	
NEXT ASST		USED ON		NEXT ASST		USED ON	
PREFERENCE		PREFERENCE		PREFERENCE		PREFERENCE	
HONEYWELL INC		HONEYWELL INC		HONEYWELL INC		HONEYWELL INC	
SILKSCREEN, CHASSIS		SILKSCREEN, CHASSIS		SILKSCREEN, CHASSIS		SILKSCREEN, CHASSIS	
SIZE 1/8" X 1/2"		SIZE 1/8" X 1/2"		SIZE 1/8" X 1/2"		SIZE 1/8" X 1/2"	
SCALE 1/1		SCALE 1/1		SCALE 1/1		SCALE 1/1	
CONTROL		CONTROL		CONTROL		CONTROL	















MOTHER BOARD  
INTERCONNECT  
LIST

ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED
GND	141-144 1-4	1-4	1-4	1-4	1-4	1-4	(J12-4)
+5V	71, 72 5-8	5-8	5-8	5-8	5-8	5-8	(J12-5)
+5V Batt.	137-140 9, 10						
SW00	12					12	
SW01	14					14	
SW02	13					13	
SW03	11					11	
SW04	24					24	
SW05	27					27	
SW06	68					68	
SW07	26					26	
SW08	76					76	
SW09	89					89	
SW10	56					56	
SW11	53					53	
SW12	67					67	
SW13	84					84	
SW14	91					91	
SW15	70					70	
Flag 0	15						
MDO00	35	35				35	
MDO01		49				49	
MDO02	17	17				17	
MDO03	21	21				21	
MDO04	42	42				42	
MDO05	45	45				45	
MDO06	18	18				18	
MDO07	22	22				22	
MDO08	25	25				25	
MDO09	38	38				38	
MDO10	46	46				46	
MDO11	55	55				55	
MDO12	28	28				28	
MDO13	39	39				39	
MDO14	48	48				48	
MDO15	57	57				57	
-12V	31/32	31/32				31/32	(J12-3)
ODIS	44	44					
EXHOLD	122	121					

MOTHER BOARD INTERCONNECT LIST								
ORIGINAL NAME		CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED
ADX00	63	63		63	63	63		
ADX01	86	86		86	86	86		
ADX02	88	88		88	88	88		
ADX03	85	85		85	85	85		
ADX04	64	64		64	64	64		
ADX05	62	62		62	62	62		
ADX06	65	65		65	65	65		
ADX07	66	66		66	66	66		
ADX08	60	60		60	60	60		
ADX09	50	50		50	50	50		
ADX10	77	77		77	77	77		
ADX11	103	103		103	103	103		
ADX12	78	78		78	78	78		
ADX13	81	81		81	81	81		
ADX14	82	82		82	82	82		
ADX15	83	83		83	83	83		
CS0*	61	61						Not Wired to DAYNL card
DSLCT	69			92		92		Tie to CPU, RDMF (92)
Flag 12								
CS1	79							Tie down (GND)
CS2	80							Tie Down (GND)
R/W*	87	87						
SEL	90							
RDMF	92			92		92		Tie also to CPU, DSLCT (69)
WRMF	93			93				
RDPF	94			94		94		
WRPF	95			95	95	95		Tie also to DEBUG, WRP (95)
F8	96				96	96		
HLT*	97					97		
BDOENA*	98	98						
F15								
CPINT	101	101				101		
F11	102				102			
C1	104							
CLK81	105			105		105		
DISTR*	106							
INCTCL		90				90		
C3B*								
C45	109			109	109	109		
CPINP	110					110		
F14	111							
EXEC	112	112				112		Called START on DAYNL
Power On*	113							Tie low
F13	114				114			

MOTHER BOARD  
INTERCONNECT  
LIST

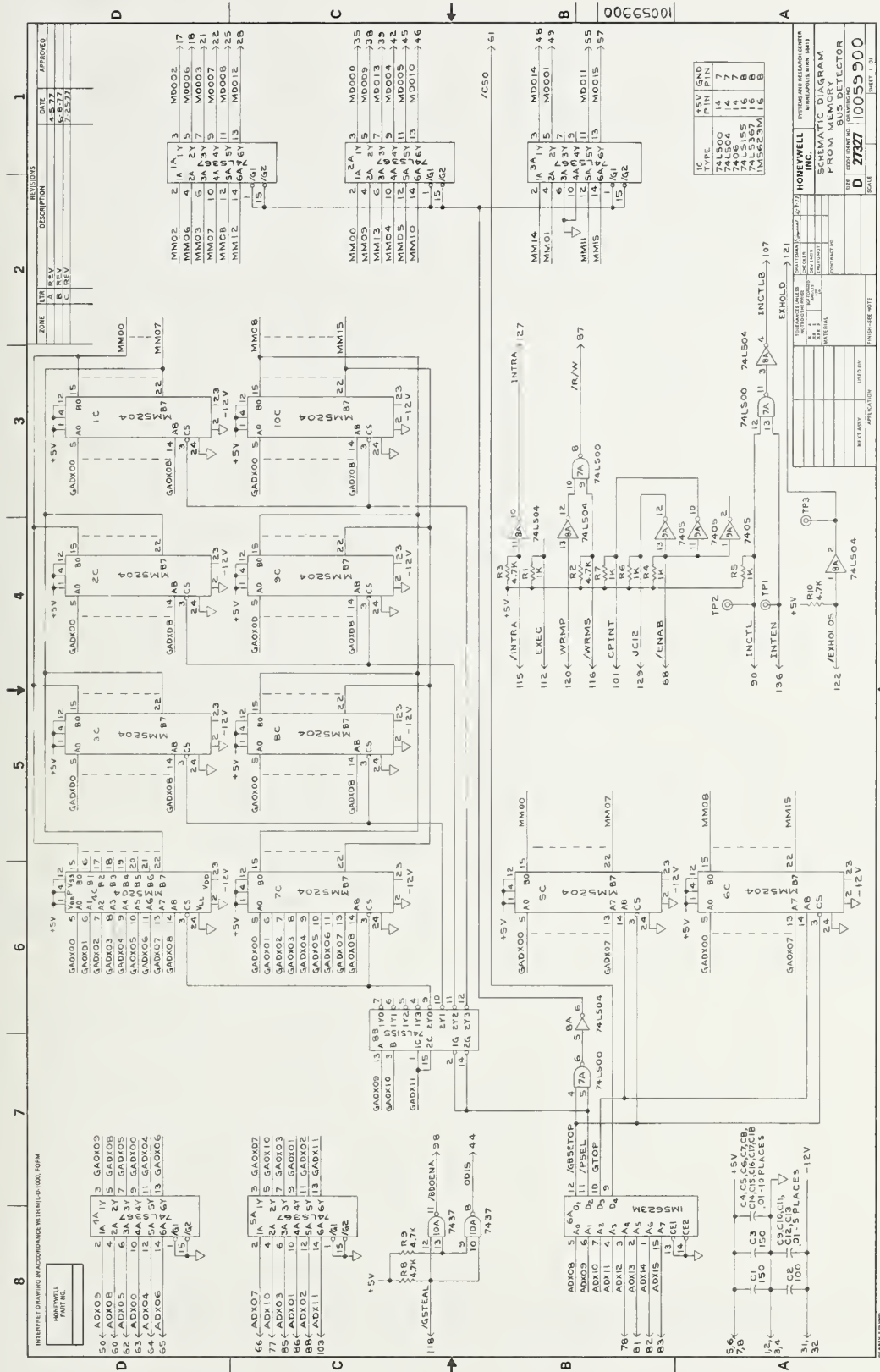
ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED
WRPA	118						
C3	100						
INCTCLB	107	107					Called INCTCL on CPU
CLK	119						
WRMP	120	120					
CLK*	121		121				
EXHOLDS*		121	122				
RFREQ	123						Tie Low
RFSH	124						
WRPB	125						
CO	126						Connect to CPU CIN (128)
INTRA	127	127					
CIN	128						Connect to CPU CO (126)
JC12	129	129					
JC13	130						Tie Low
JC15	131				131		
F12							
JC14	133				133		
SYSCLR*	134				134		
INIT*	135				135	135	
INTEN	136	136				136	
BDO00	36		36	36	36		
BDO01	40		40	40	40		
BDO02	58		58	58	58		
BDO03	20		20	20	20		
BDO04	43		43	43	43		
BDO05	54		54	54	54		
BDO06	19		19	19	19		
BDO07	23		23	23	23		
BDO08	37		37	37	27		
BDO09	41		41	41	41		
BDO10	51		51	51	51		
BDO11	52		52	52	52		
BDO12	74		74	74	74		
BDO13	73		73	73	73		
BDO14	47		47	47	69		
BDO15	59		59	59	59		
PPSTL*			24				
GMDTAD*		25	25				
GMMADDD*		113	113				
GSTRTCV*		31	31				
GMEMLWRD*		111	111				
GMFMUPRD*		107	107				
GMARD*		104	104				
GCLKSTB*		28	28				
GMEMDEST*		30	30				
GMEMSRC*		32	32				

MOTHER BOARD INTERCONNECT LIST							
ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED
GMEMUPRS*			34	34			
GADCONV*			29	29			
GMEMLWRS*			35	35			
GINCMAR*			106	106			
GDECMAR*			108	108			
GMARS*			110	110			
LSIGHI 1				9			To Connector J5- 4
LSIGHI 2				13			To Connector J5- 3
LSIGHI 3				10			To Connector J5- 2
LSIGHI 4				14			To Connector J5- 1
LSIGHI 5				46			To Connector J4- 4
LSIGHI 6				55			To Connector J4- 3
LSIGHI 7				67			To Connector J4- 2
LSIGHI 8				68			To Connector J4- 1
LSIGHI 9				87			To Connector J3- 4
LSIGHI 10				90			To Connector J3- 3
LSIGHI 11				96			To Connector J3- 2
LSIGHI 12				97			To Connector J3- 1
LSIGHI 13				117			To Connector J2- 4
LSIGHI 14				123			To Connector J2- 3
LSIGHI 15				125			To Connector J2- 2
LSIGHI 16				127			To Connector J2- 1
LSIGLO 1				11			To Connector J5- 17
LSIGLO 2				15			To Connector J5- 16
LSIGLO 3				12			To Connector J5- 15
LSIGLO 4				16			To Connector J5- 14
LSIGLO 5				48			To Connector J4- 17
LSIGLO 6				57			To Connector J4- 16
LSIGLO 7				69			To Connector J4- 15
LSIGLO 8				70			To Connector J4- 14
LSIGLO 9				89			To Connector J3- 17
LSIGLO 10				91			To Connector J3- 16
LSIGLO 11				98			To Connector J3- 15
LSIGLO 12				99			To Connector J3- 14
LSIGLO 13				119			To Connector J2- 17
LSIGLO 14				124			To Connector J2- 16
LSIGLO 15				126			To Connector J2- 15
LSIGLO 16				128			To Connector J2- 14
PGS*							
/PPSTLP			112	112			
BPPD0			46	45			
BPPD1			50	49			
BPPD2			53	53			
BPPD3			56	56			
BPPD4			61	61			
BPPD5			75	75			



MOTHER BOARD INTERCONNECT LIST							
ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED
BPPD6			76	76			
BPPD7			79	79			
BPPD8			80	80			
BPPD9			100	100			
BPPD10			101	102			
BPPD11			102	101			
ENAB*		68				69	Gnd by DAYNL
INTRA*		115		115			
WRMS*		116		116			
ASC2*							
CS0*							Not wired to CPU
CS2*							Tied High
CS1*							Tied High
CS3*							
RDM						92	Connect to CPU, RDMF (92)
RDP							Connect to CPU, RDPF (94)
WRP						95	Connect to CPU, WRPF (95)
START							Connect to CPU, EXEC (112)
+15V				18	18		J12-15
-15V				136			J12-6
GNRLCLR*			17				
S1				129			To Front Panel (J12-8)
S1*				130			To Front Panel (J12-10)
S2				132			To Front Panel (J12-7)
S2*				136			To Front Panel (J12-9)
OV1				21			To Connector J5-25
OV2				22			To Connector J5-22
OV3				24			To Connector J5-11
OV4				25			To Connector J5-10
OV5				48			To Connector J4-25
OV6				46			To Connector J4-22
OV7				45			To Connector J4-11
OV8				44			To Connector J4-10
OV9				99			To Connector J3-25
OV10				100			To Connector J3-22
OV11				104			To Connector J3-11
OV12				105			To Connector J3-10
OV13				127			To Connector J2-25
OV14				128			To Connector J2-22
OV15				121			To Connector J2-11
OV16				122			To Connector J2-10
OB1				26			To Connector J5-12
OB2				27			To Connector J5-13
OB3				28			To Connector J5-24
OB4				29			To Connector J5-23
OB5				42			To Connector J4-12

MOTHER BOARD INTERCONNECT LIST							
ORIGINAL NAME	CPU	P. MEM	PREPROCESSOR #1	PREPROCESSOR #2	I/O	DEBUG	NOT USED
OB6					39		To Connector J4-13
OB7					38		To Connector J4-24
OB8					35		To Connector J4-23
OB9					106		To Connector J3-12
OB10					107		To Connector J3-13
OB11					108		To Connector J3-24
OB12					110		To Connector J3-23
OB13					119		To Connector J2-12
OB14					120		To Connector J2-13
OB15					117		To Connector J2-24
OB16					118		To Connector J2-23
ANALOG GND							From Power Supply (J12)
/GFAULT 1					113		CR1 & J12-14
/GFAULT 2					112		CR2 & J12-12
/GFAULT 3							CR3 & J12-2
/EXT RESET					111		To Connector J12-13
LOGIC GND							To Connector J12-1
/GSTEAL							
SIG SHIELD		118		118			To Connector Pins J2-5 J3-5, J4-5, J5-5





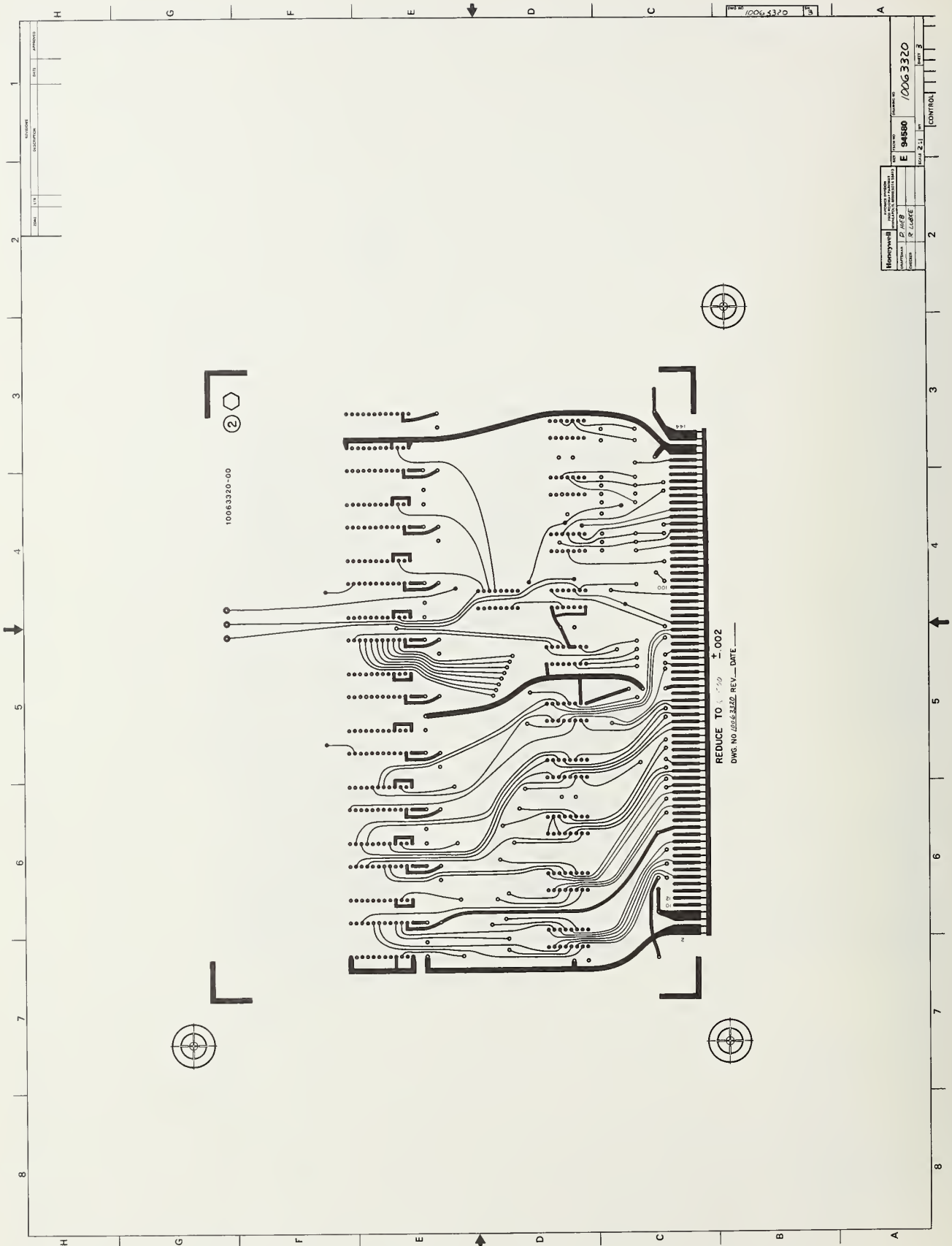


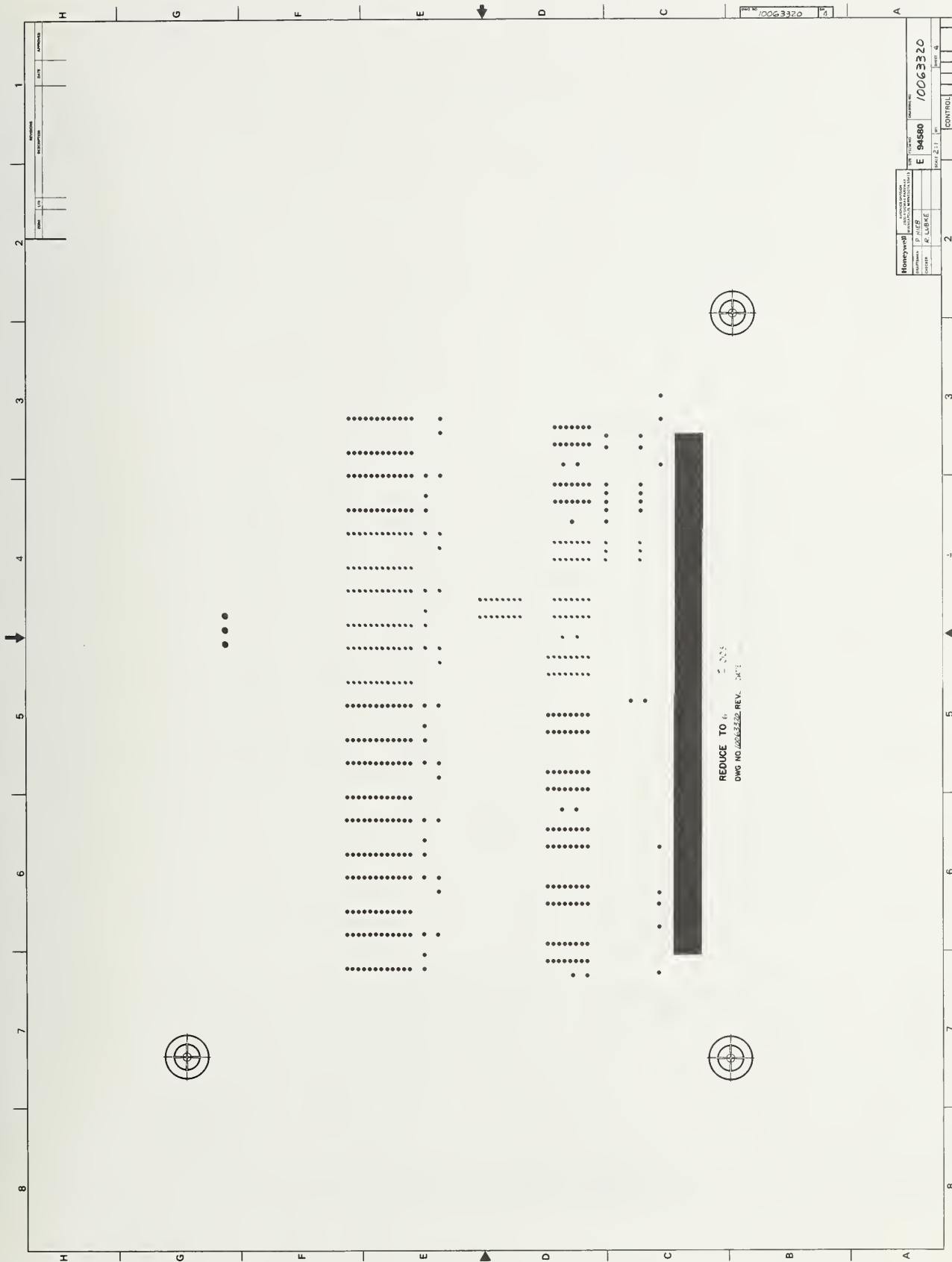














# Honeywell

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SUPERSEDES SUPERSEDED BY						ENGINEERING PARTS LIST							
REV.	DATE	E.O.	REV.	DATE	E.O.	BUS DETECTOR, I/O						10059899	
						TYPED BY	PRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.		
A	2 Mar 77									2	1		
	6-9-77												
PART NO.						PART NAME						QTY	
74LS174						Hex D Register						6	1B, 2B, 3B, 4B, 5B, 6B
7407						Hex OC Buffer						6	1A, 2A, 3A, 4A, 5A, 6A
74LS00						Quad NAND						2	8A, 10A
74LS74						DUAL D FLIP FLOP						2	8D, 9A
74LS221						DUAL MONOSTABLE FF						2	6D, 7A
74LS02						QUAD NOR						3	7D, 9B, 10C
74LS04						HEX INVERTER						1	7B
74LS138						1 OF 8 DECODER						2	8C, 9C
7425						DUAL 4 NOR						1	8A
7406						HEX OC INVERTER						1	9D
CD4023						TRIPLE NAND						1	6C
CD4009						HEX INVERTER						1	10D
74LS27						TRIPLE 3 NOR						1	7C
LM211D						COMPARATOR						1	4C
T8201						SWITCH SPDT						2	SW1, 3
B8600						" SPST MOM						1	SW2
RCR07G621JF						RESISTOR, 620 $\Omega$ , 1/4W						1	R10
RCR07G243JF						" , 24K, "						1	R11
RCR07G100JF						" , 10K, "						2	R1, 12
RCR07G104JF						" , 100K, "						3	R13, 14, 18
RCR07G393JF						" , 39K, "						1	R22
RCR07G274JF						" , 270K, "						1	R16
RCR07G514JF						" , 510K, "						1	R19

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SUPERSEDED BY

## ENGINEERING PARTS LIST

SUPERSEDES						ENGINEERING PARTS LIST									
SUPERSEDED BY															
REV.	DATE	E.O.	REV.	DATE	E.O.	BUS DETECTOR, I/O				10059899					
						TYPED BY	PRPD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.				
	29 Mar-77									2	2				
A	6-7-77														
B	7-27-77														
C	9-8-77														
D	10-6-77														
PART NO.		PART NAME				QTY									
RCR07G47ZJP		RESISTOR, 4.7K 1/4W				4	R7,8,	9,20,21							
3389H		POTENTIOMETER, 50K				1	R24				BOURNS				
3389H		" , 100K				1	R23				BOURNS				
RCR07G102JP		RESISTOR, 1K, 1/4 W				4	R3,	4,5,6							
IN914		DIODE				3	CR2,	3,4							
IN 821		DIODE, ZENER				1	CR1								
CK06BX105K		CAPACITOR, 1μf				4	C8,	17,18,20							
CK05BX102K		" , .001				2	C7,	14							
TGS10		" , .01				10	C1,5,	6,9,10,11,12,13,15,16			SPRAGUE				
CK05BX100K		" , 10pf				1	C3								
M39003/01-2295		" , 47μf				1	C19				ALT: 10029798-169				
M39003/01-2277		" , 150μf				2	C2,4				ALT: 10029798-128				
74LS73		DUAL J-K FF				1	I0B								
RCR07G822JP		RESISTOR, 82K				1	R2								
448934-7		TERMINAL				4	TP1,	2,3,4			ALT: 15122 CAMBION				
10063321		PC BOARD				1									

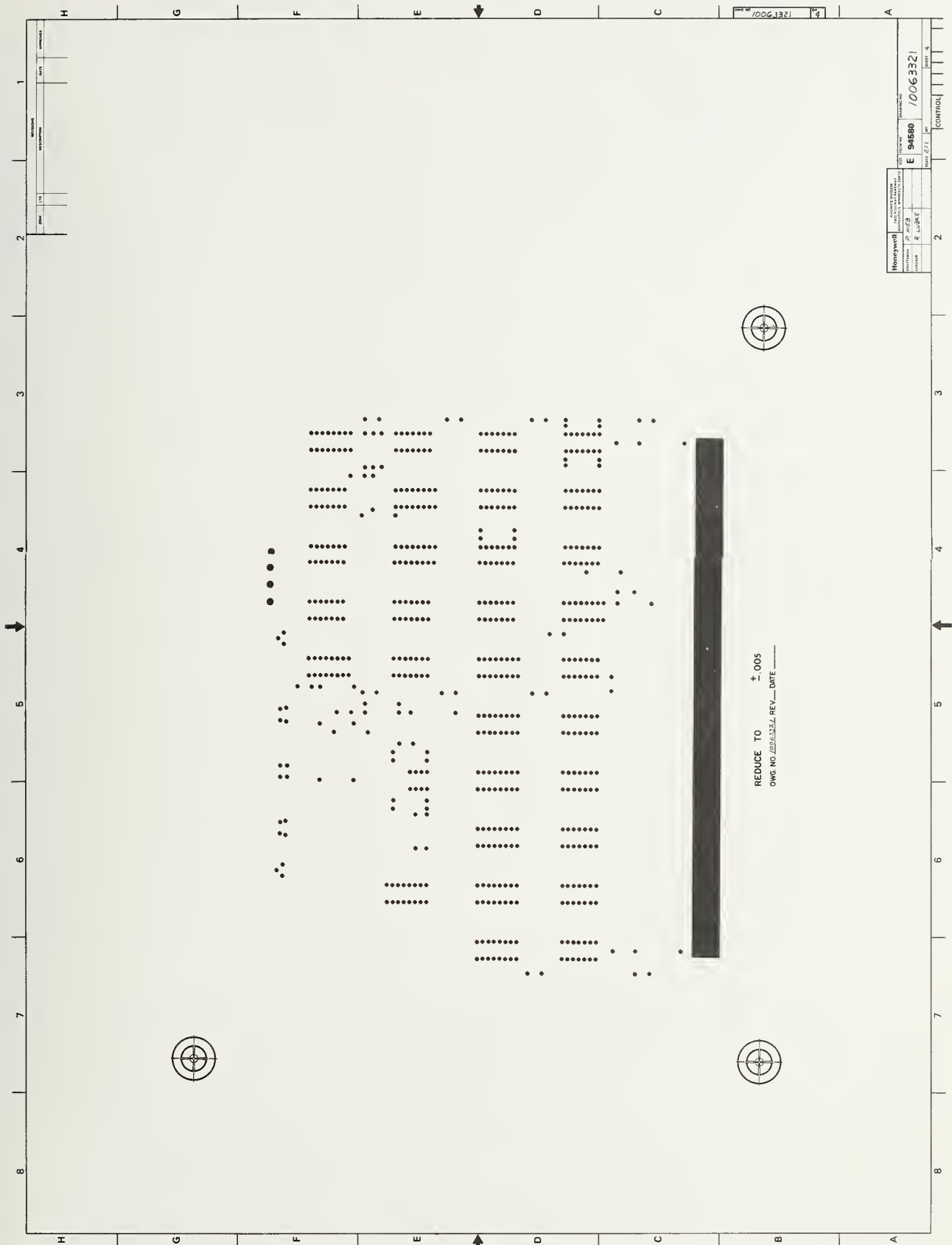


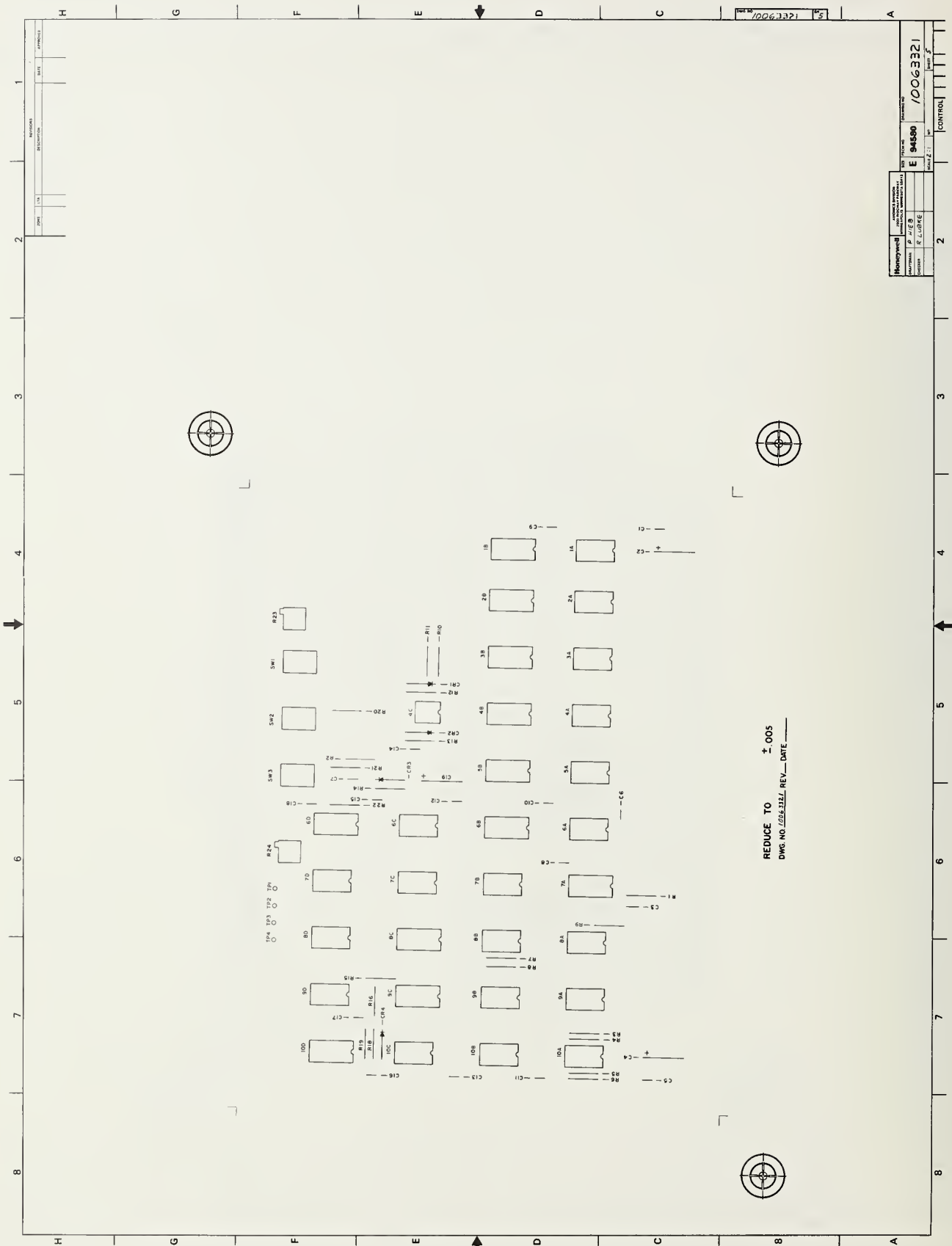










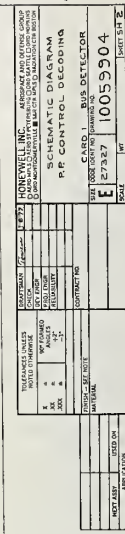


REDUCE TO 1/8" ± .005  
DWS NO. 1006332/ REV. DATE

Honeywell		Control Panel	
Part No.	1006332	Rev.	1
Manufacturer	P. J. E. B.	Customer	E. 94580
Control	R. L. G. B. E.	Control	1006332
CONTROL		CONTROL	







Honeywell

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SUPERSEDES SUPERSEDED BY						ENGINEERING PARTS LIST							
						P.P. CONTROL DECODING CARD 1				10059909			
REV.	DATE	E.O.	REV.	DATE	E.C.	TYPED BY	PRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.		
A	6-10-77									2	1		
B	7-28-77												
PART NO.						PART NAME							
						QTY							
7400						QUAD 2 NAND	1	2F					
74LS00						QUAD 2 NAND	3	4E, 9D, 11E					
74LS02						QUAD 2 NOR	3	1D, 9F, 11D					
7404						HEX INVERTER	1	5D					
74LS04						HEX INVERTER	6	1E, 2C, 7C, 7D, 8C, 10E					
7406						HEX OC INV	1	4F					
74LS08						QUAD 2 AND	2	2E, 7E					
74LS10						TRIPLE 3 NAND	1	6D					
74LS11						TRIPLE 3 AND	1	2D					
74LS27						TRIPLE 3 NOR	1	8F					
74LS30						8 NAND	1	8D					
74S140						DUAL 4 IN POS NAND	1	1F					
74LS37						QUAD 2 BUF NAND	1	9E					
74LS74						DUAL D FF	3	3F, 3E, 8E					
74LS138						3 TO 8 DECODER	3	2A, 6C, 9C					
74LS154						4 TO 16 DEC/DEM	2	3A, 4A					
74LS163						SYNC 4-BIT COUNT	2	5E, 6E					
74LS174						HEXQUAD D-FF	4	5A, 6A, 10A, 11A					
74LS175						HEXQUAD D-FF	3	3D, 4D, 10F					
74LS181						ALU	3	7A, 8A, 9A					
74LS194						4-BIT SHIFT REG.	2	1B, 1C,					
74LS197						BIN COUNTER/LATCH	2	3C, 4C,					
74LS251						DATA SEL/MULTIPLEX	1	11F					
74LS367						HEX BUS DRIVERS	5	5B, 5C, 10C, 11B, 11C					

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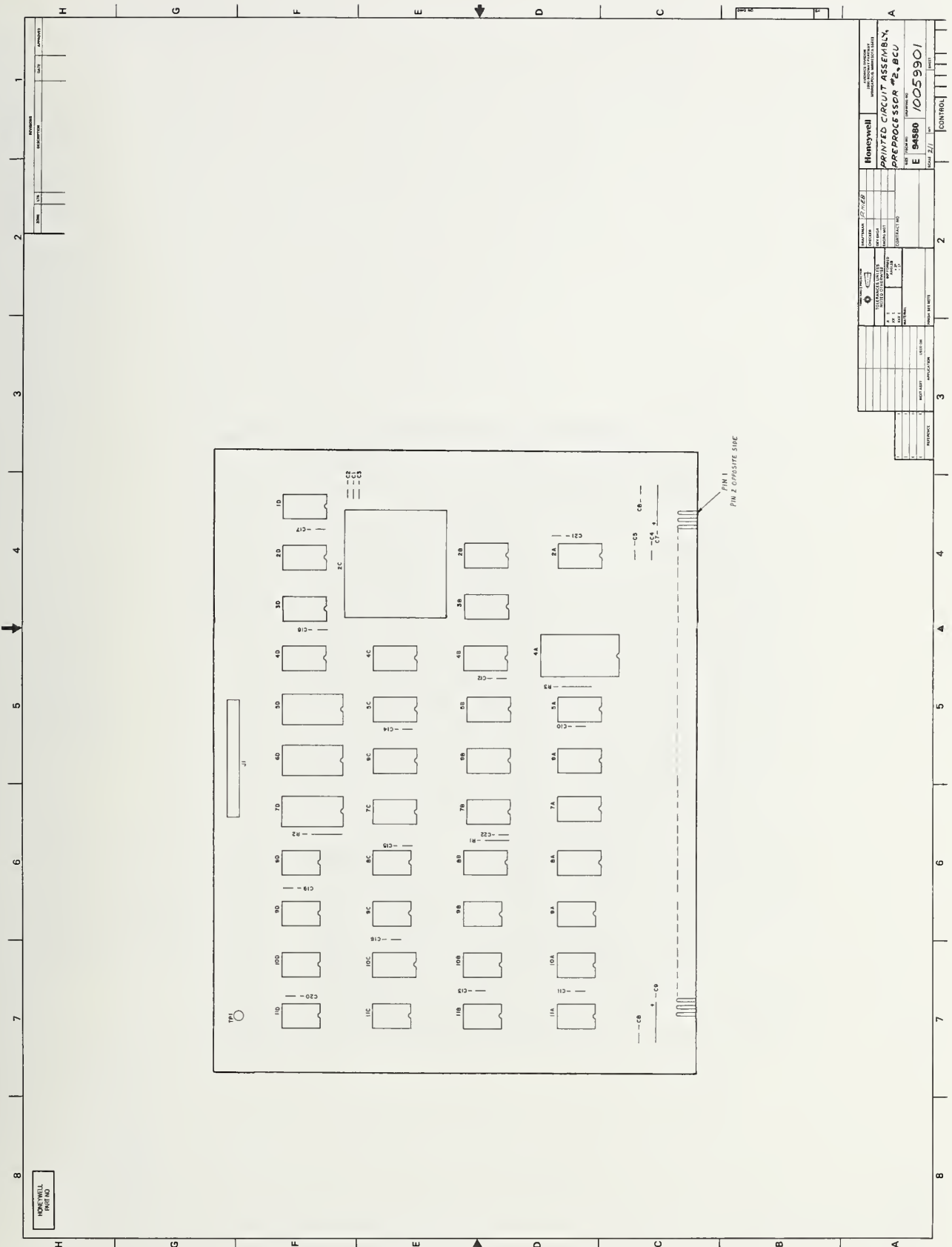


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SUPERSEDES SUPERSEDED BY						ENGINEERING PARTS LIST													
REV.	DATE	E.O.	REV.	DATE	E.O.	CYCLE STEAL CONTROL ADDRESS PREPROCESSOR CARD 2				10059901									
A	7-12-77		B	7-21-77		TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.								
C	10-6-77									1	1								
PART NO.						PART NAME						QTY							
74LS00	QUAD 2 NAND					1	9D												
74LS02	QUAD 2 NOR					3	10B, 8C, 8D												
74S04	HEX INVERTER					1	11A												
74LS04	HEX INVERTER					2	10A, 9C												
74LS08	QUAD 2 AND					1	11C												
74LS27	TRIPLE 3 NOR					1	9A												
7437	QUAD 2 BUF NAND					1	11B												
74LS74	DUAL D FF					2	11D, 9B												
74LS157	QUAD 2 MULT					1	5C												
74LS164	8BIT SHIFT REG.					1	10D												
74LS174	HEX QUAD D-FF					4	8B, 6B, 5B, 2B												
74LS193	4BT UP/DN COUNTER					2	7C, 4B												
74LS367	HEX BUS DRIVERS					14	10C, 8A, 7A, 7B, 6A, 6C, 5A, 4C, 4D, 2A, 3B, 3D, 2D, 1D												
2101A	256x4 RAM					3	7D, 6D, 5D				INTEL								
IH5060	16-Channel MLIX					1	4A				INTERSEIL								
ADC-EH8B1	A/D Converter					1	2C				DATTEL								
RCR07G102JP	RESISTOR, 1K, 1/4W					3	R1, 2, 3												
TGS10	CAPACITOR, .01μF					14	C8 THRU 21				SPRAGUE								
CK06BX104K	CAPACITOR, 1μF					5	C1, 2, 3, 4, 5												
M39003/01-2277	CAPACITOR, 150μF					2	C6, 7				ALT: 10029798-128								
3432-1002	CONNECTOR					1					3M								
10063323	PC BOARD					1													

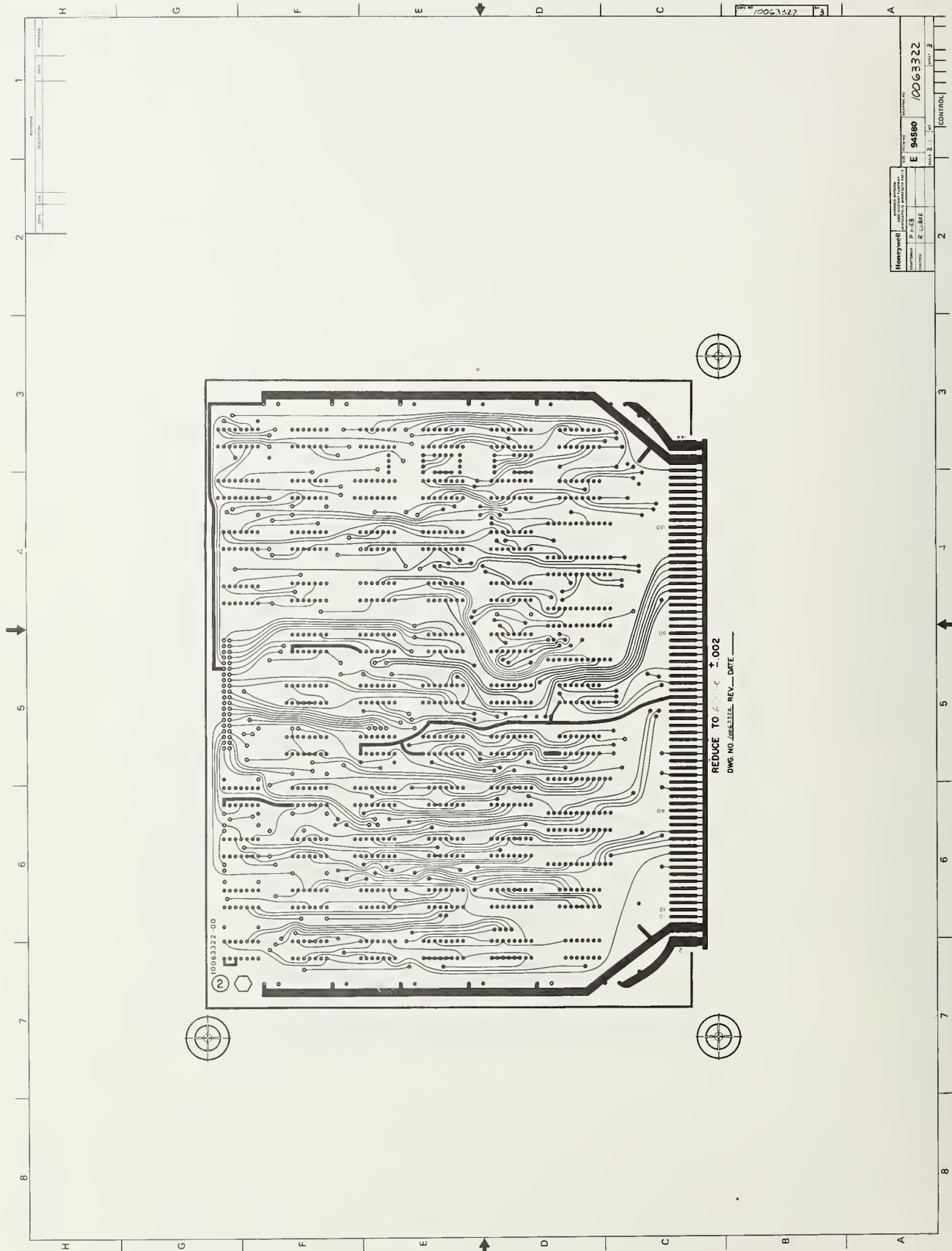
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<b>Heaterprint</b> Part No. <b>E 94580</b> Rev. <b>1.0</b> Date <b>10/06/3322</b>		Sheet <b>2</b> of <b>3</b> Control
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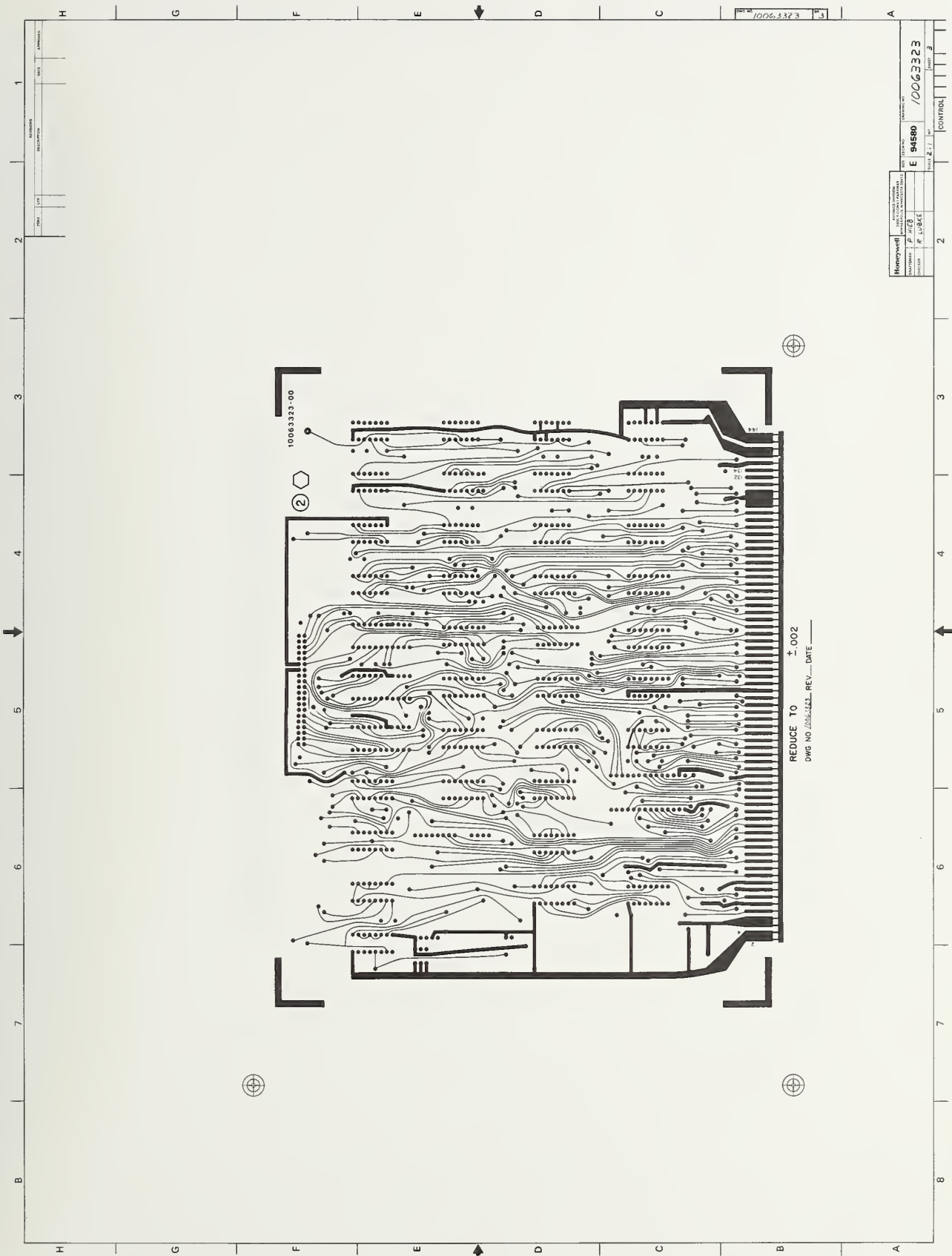


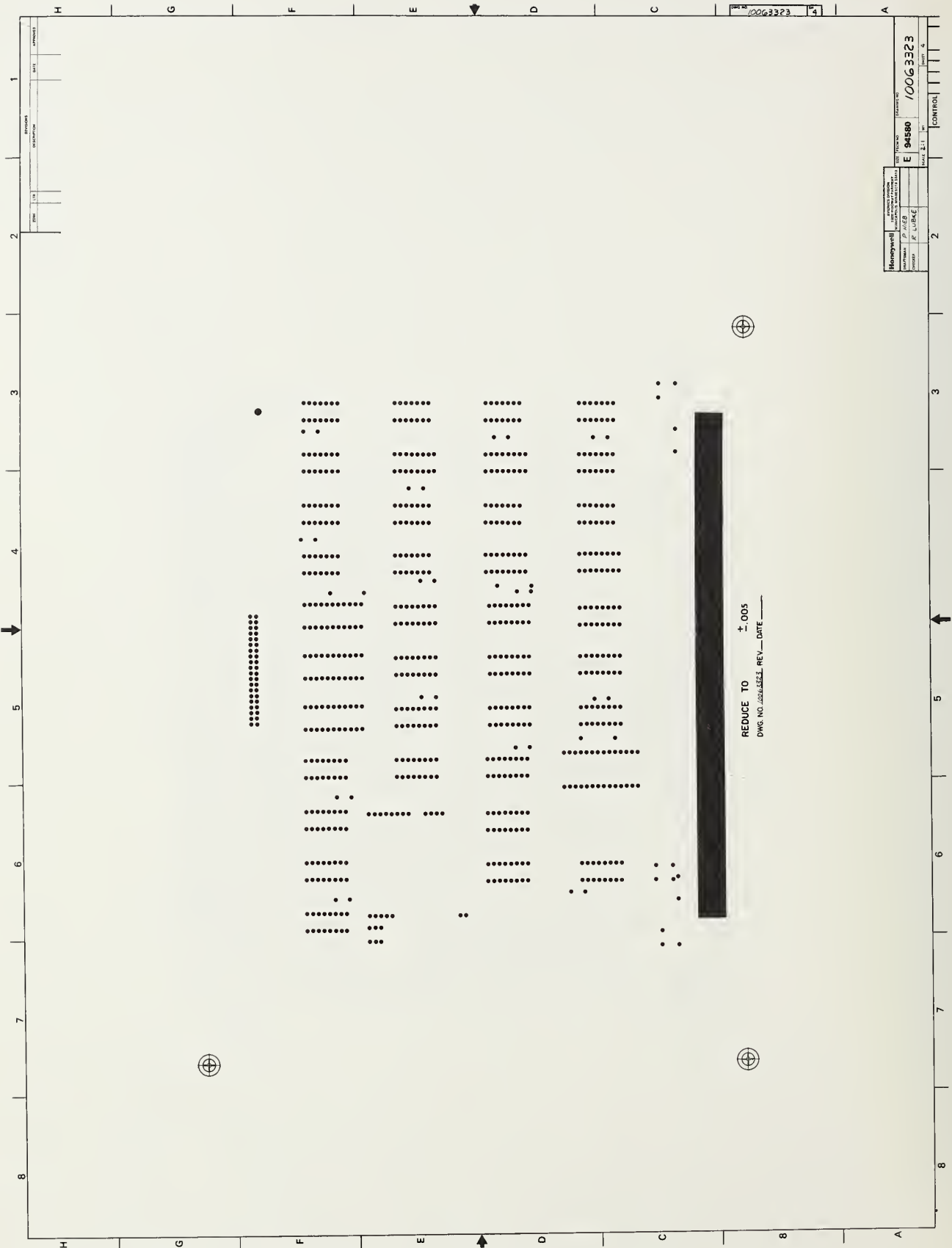












REDUCE TO 1/4" = 1'-0"  
 DWS NO. 10063323 REV. DATE

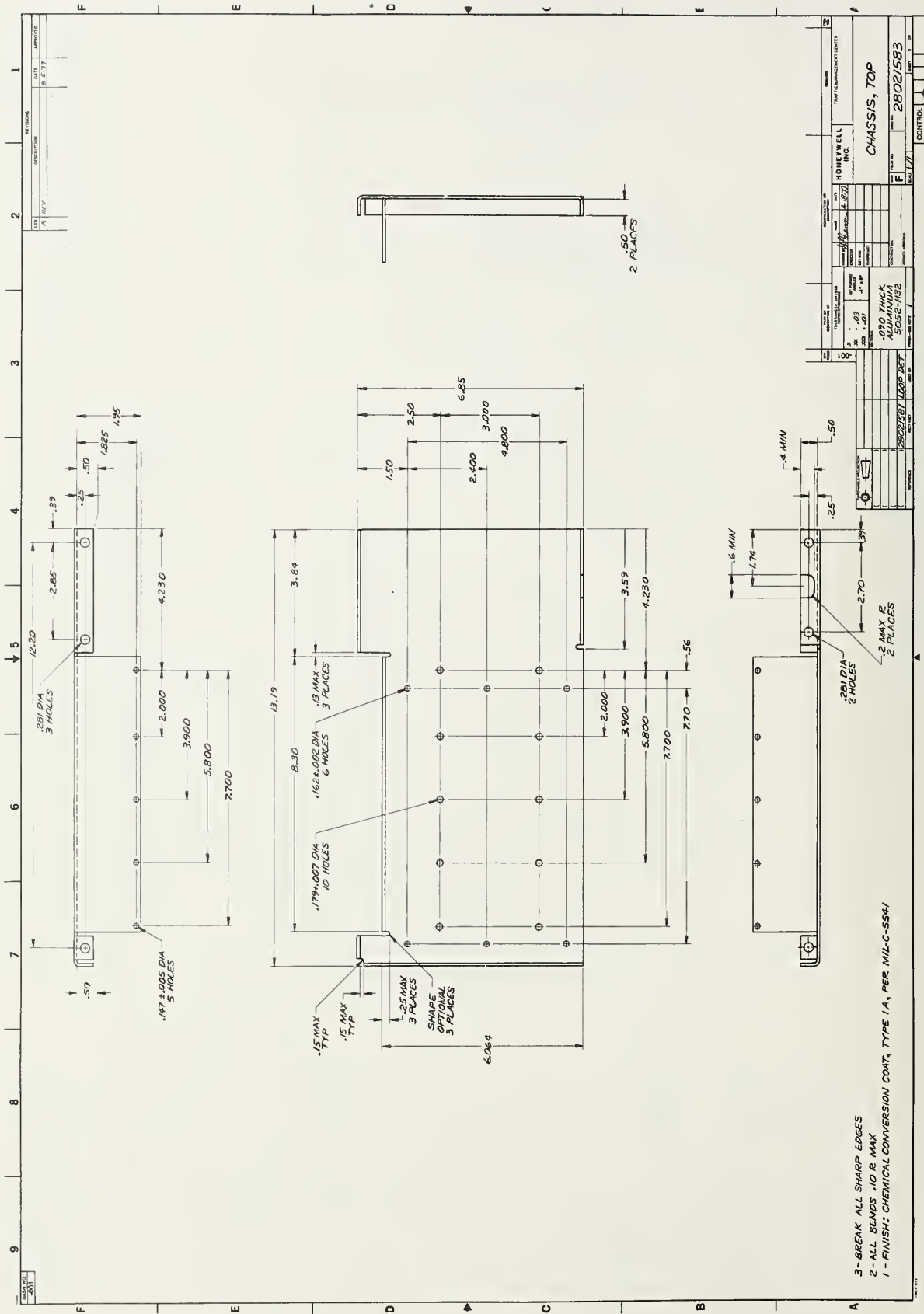
HONEYWELL AUTOMATICALLY REPRODUCED FROM THE ORIGINAL DRAWING		E 94580 10063323	10063323 10063323
CONTROL		10063323	10063323

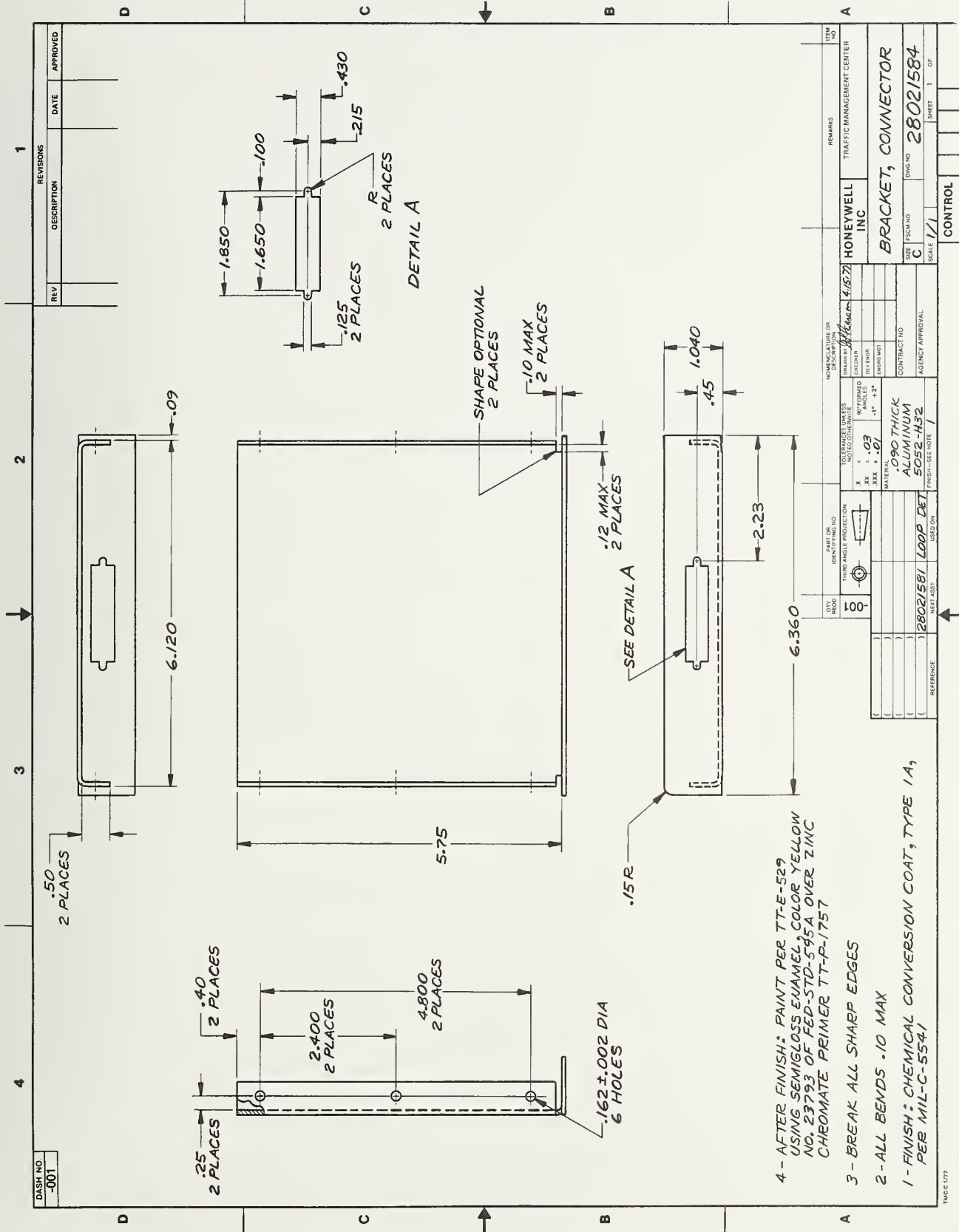










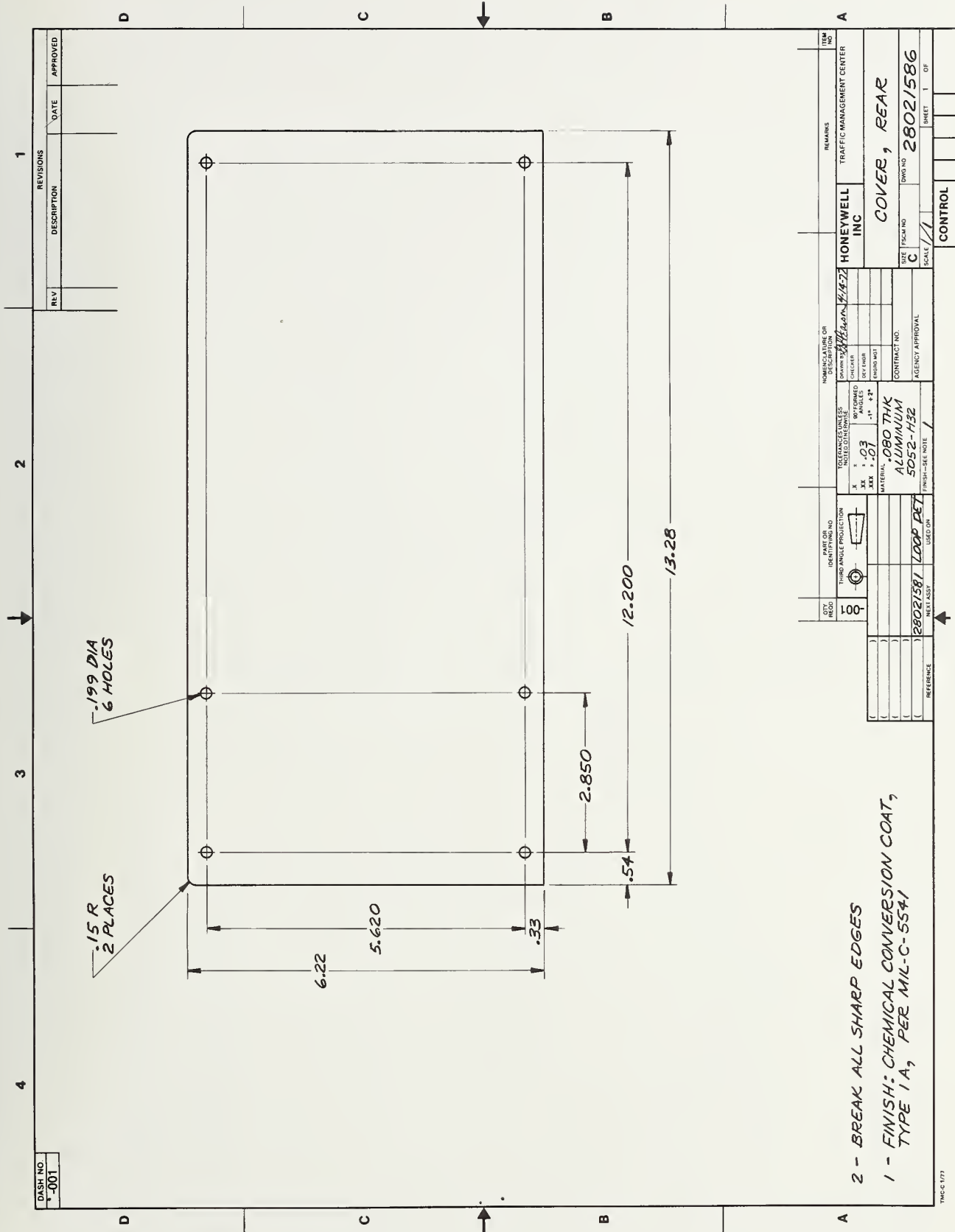


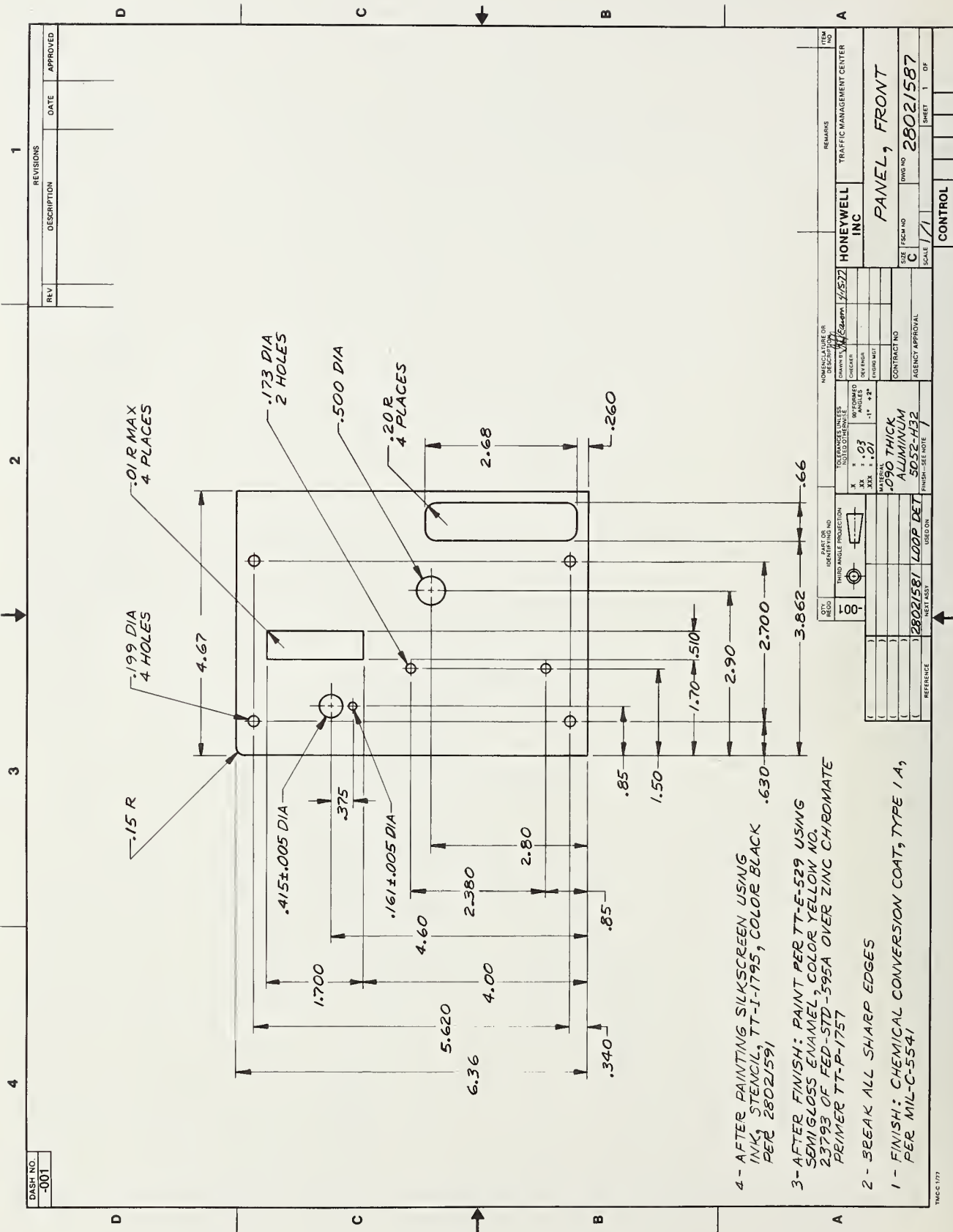
- 4 - AFTER FINISH: PAINT PER TT-E-539 USING SEMI-GLOSS ENAMEL, COLOR YELLOW NO. 23793 OF FED-STD-595A OVER ZINC CHROMATE PRIMER TT-P-1757
- 3 - BREAK ALL SHARP EDGES
- 2 - ALL BENDS .10 MAX
- 1 - FINISH: CHEMICAL CONVERSION COAT, TYPE 1A, PER MIL-C-5541

DASH NO. -001		REV. NO.		DESCRIPTION		DATE		APPROVED	
QTY. 100		PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		REMARKS		ITEM NO.	
THIRD ANGLE PROJECTION		DRAWN BY HONEYWELL INC.		CHECKED BY HONEYWELL INC.		TRAFFIC MANAGEMENT CENTER		HONEYWELL INC.	
MATERIAL ALUMINUM 5052-H32		NOTED DIMENSIONS X .03 X .01 X .01		NOTED DIMENSIONS X .03 X .01 X .01		CONTRACT NO.		BRACKET, CONNECTOR	
NEXT ASSY 28021581 LOOP DET		USED ON		AGENCY APPROVAL		SCALE 1/1		CONTROL	
REFERENCE		28021584		DOW NO.		28021584		SHEET 1 OF 1	







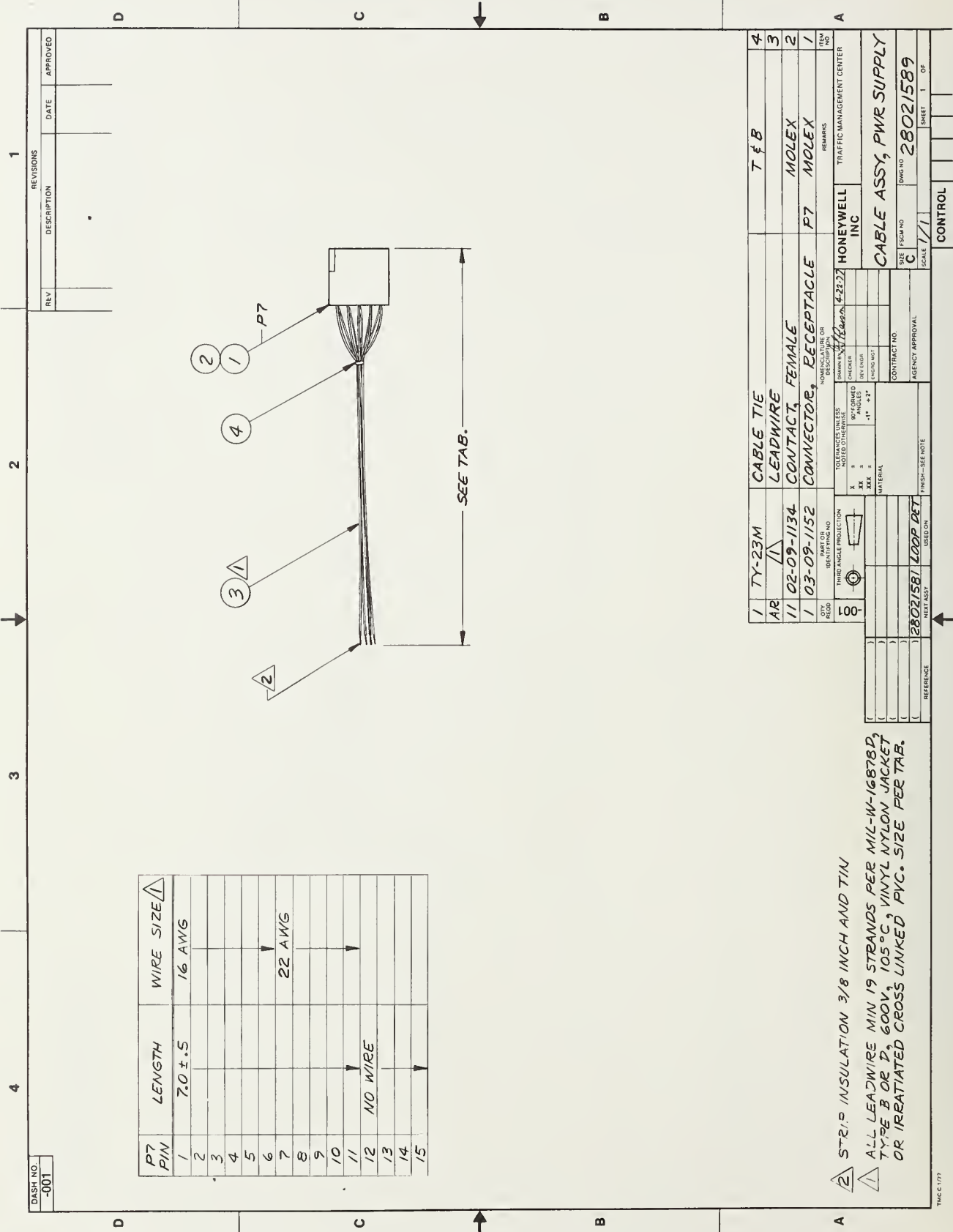


DASH NO.		REV.		REVISIONS		DATE		APPROVED	
-001									

HONEYWELL INC		REMARKS	
1/6/72		TRAFFIC MANAGEMENT CENTER	
C		SCALE 1/1	
C		DWG NO 2802/587	
C		SHEET 1 OF 1	



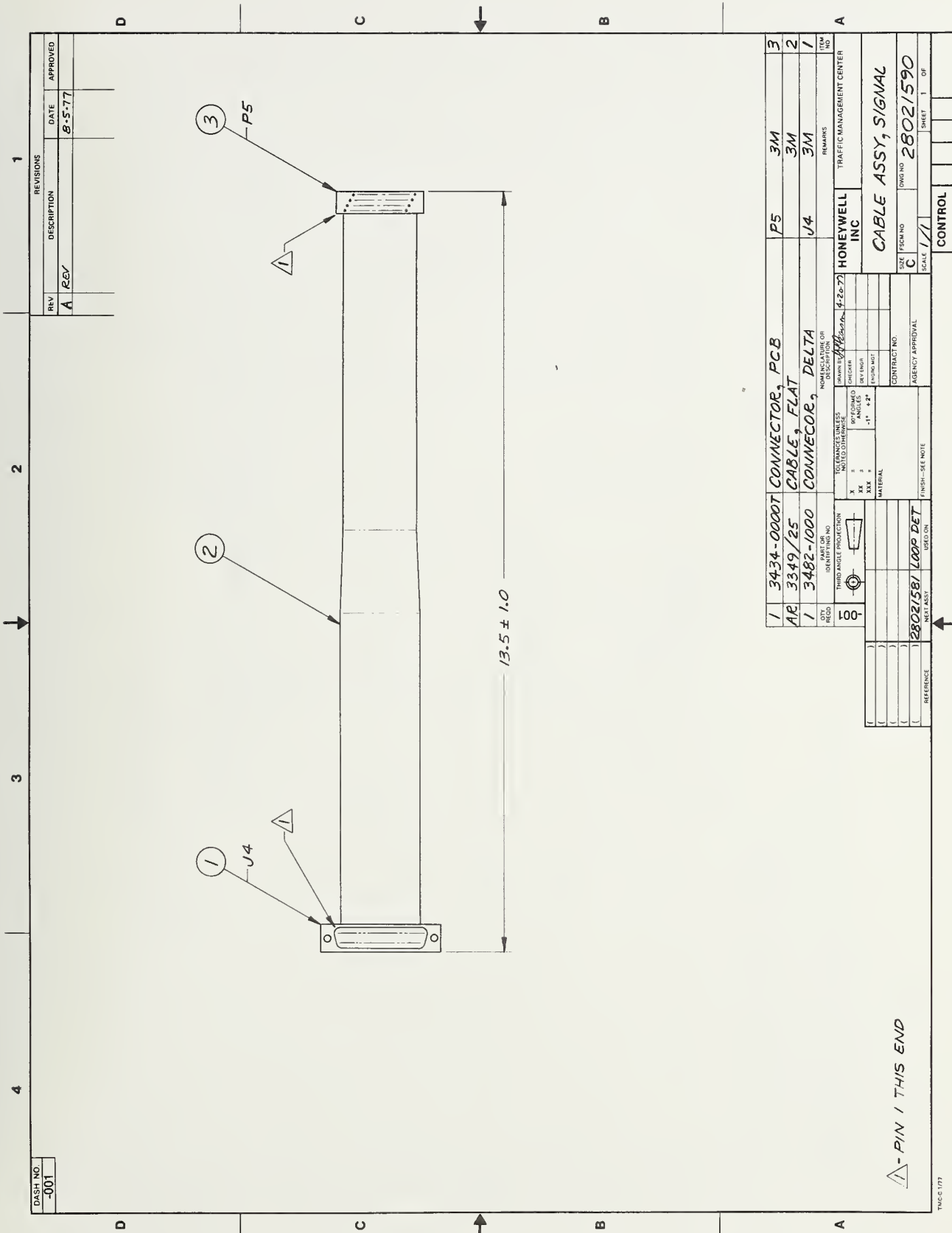


DASH NO.  
-001

REV	DESCRIPTION	DATE	APPROVED

2 STRIP INSULATION 3/8 INCH AND TIN  
 ALL LEADWIRE MIN 19 STRANDS PER MIL-W-16878D,  
 TYPE B OR D, 600V, 105 °C, VINYL NYLON JACKET  
 OR IRRADIATED CROSS LINKED PVC. SIZE PER TAB.

1	TY-23M	CABLE TIE	T & B	4
AR	11	LEADWIRE		3
11	02-09-1134	CONTACT, FEMALE	MOLEX	2
1	03-09-1152	CONNECTOR, RECEPTACLE	P7 MOLEX	1
100				
DRAWING NO. 4-22-23		HONEYWELL INC		
CHECKED BY EUG		TRAFFIC MANAGEMENT CENTER		
MATERIAL		CABLE ASSY, PWR SUPPLY		
CONTRACT NO.		28021589		
AGENCY APPROVAL		SCALE 1/1		
FINISH - SEE NOTE		CONTROL		



DASH NO  
-001

REVISIONS		
REV	DESCRIPTION	DATE
A	REV	8-5-77

1	3434-0000T	CONNECTOR, PCB	P5	3M	3
AR	3349/25	CABLE, FLAT		3M	2
1	3482-1000	CONNECTOR, DELTA	J4	3M	1
TRAFFIC MANAGEMENT CENTER					
HONEYWELL INC					
CABLE ASSY, SIGNAL					
CONTRACT NO					
AGENCY APPROVAL					
FINISH—SEE NOTE					
USED ON					
NEXT ASSY					
REFERENCE					
2802/581 LOOP DET					
SIZE TECH NO					
SCALE					
2802/590					
SHEET 1 OF					
CONTROL					

△ - PIN 1 THIS END

TWC 5 1/77

DASH NO.  
-001

MONITOR  
 SELECT  
 2 3 4  
 LOOP  
 DETECTOR

J3

REV. DESCRIPTION DATE APPROVED

HONEYWELL  
INC

REMARKS  
TRAFFIC MANAGEMENT CENTER

QTY.  
REQD  
-001

PART OR  
IDENTIFYING NO.

NOMENCLATURE OR  
DESCRIPTION  
 DRAWN BY: *W. H. H. 5-2-77*  
 CHECKER  
 DESIGNED  
 ENGR. NO.

TOLERANCES UNLESS  
NOTED OTHERWISE  
 X ± .005  
 XX ± .010  
 XXX ± .015  
 MATERIAL

THIRD ANGLE PROJECTION

FINISH—SEE NOTE  
 USED ON

REFERENCE  
 2802/587 LOOP DET

CONTRACT NO.

AGENCY APPROVAL

SIZE  
B

FSCM NO.

DWG NO. 2802/591

SCALE 1/1

CONTROL

SHEET 1 OF

TMC 8 1/77





二

TMC-A 1/77

CONTROL





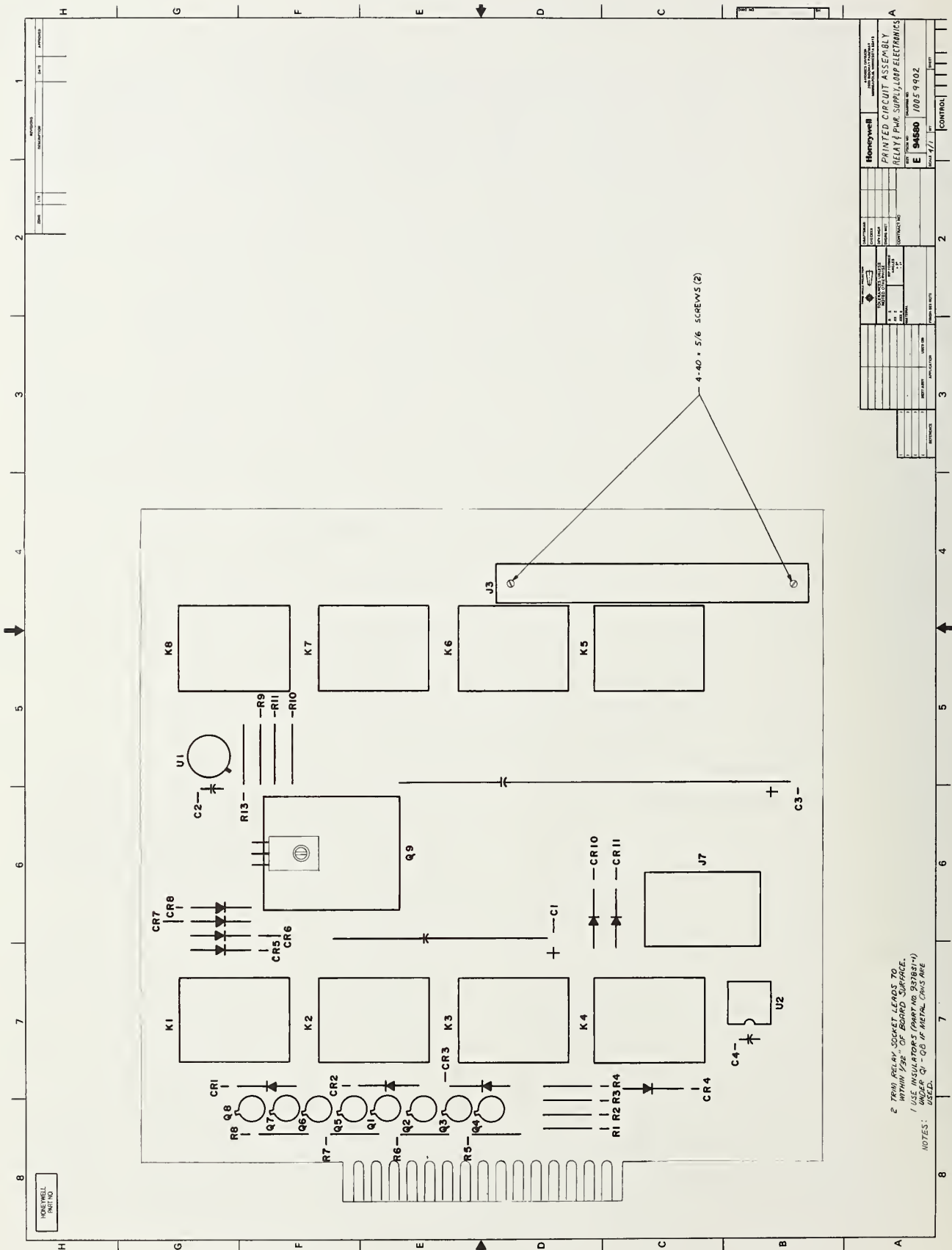
# Honeywell

PRINTED IN U. S. A.

SUPERSEDES SUPERSEDED BY						ENGINEERING PARTS LIST				10059902	
REV.	DATE	E. O.	REV.	DATE	E. O.	POWER SUPPLY LOOP ELECTRONICS				SHEETS	SHEET NO.
A	7-12-77					TYPED BY	PRD. BY	CHKD. BY	DATE	1	1
B	7-29-77										
C	10-6-77										
D	10-10-77										
PART NO.						PART NAME					
CA3130						OP AMPL					
723L						VOLTAGE REG					
2N2222						TRANSISTOR					
2N5298						TRANSISTOR					
1N4384						RECTIFIER					
1N4454						DIODE					
RCR07G391J						RESISTOR 390					
RCR07G103J						RESISTOR 10K					
RCR20G1R0J						RESISTOR 1					
RN55D6801F						RESISTOR 681					
RN55D1001F						RESISTOR 1K					
CM04ED101J						CAPACITOR 100pF					
501U025DIN						CAPACITOR 500					
232U050N3C						CAPACITOR 2300					
AZ420-V50-4H						RELAY					
ST140-A1						RELAY SOCKET					
ST140-1						RETAINER					
205859-2						CONNECTOR, RTANG					
03-09-2153						PLUG					
02-09-2134						CONTACT, MALE					
6-32UNCx.38LG						SCREW, PAN HEAD					
NO. 6						LOCKWASHER					
6-32						NUT, HEX					
10063315						PC BOARD					

HE-124



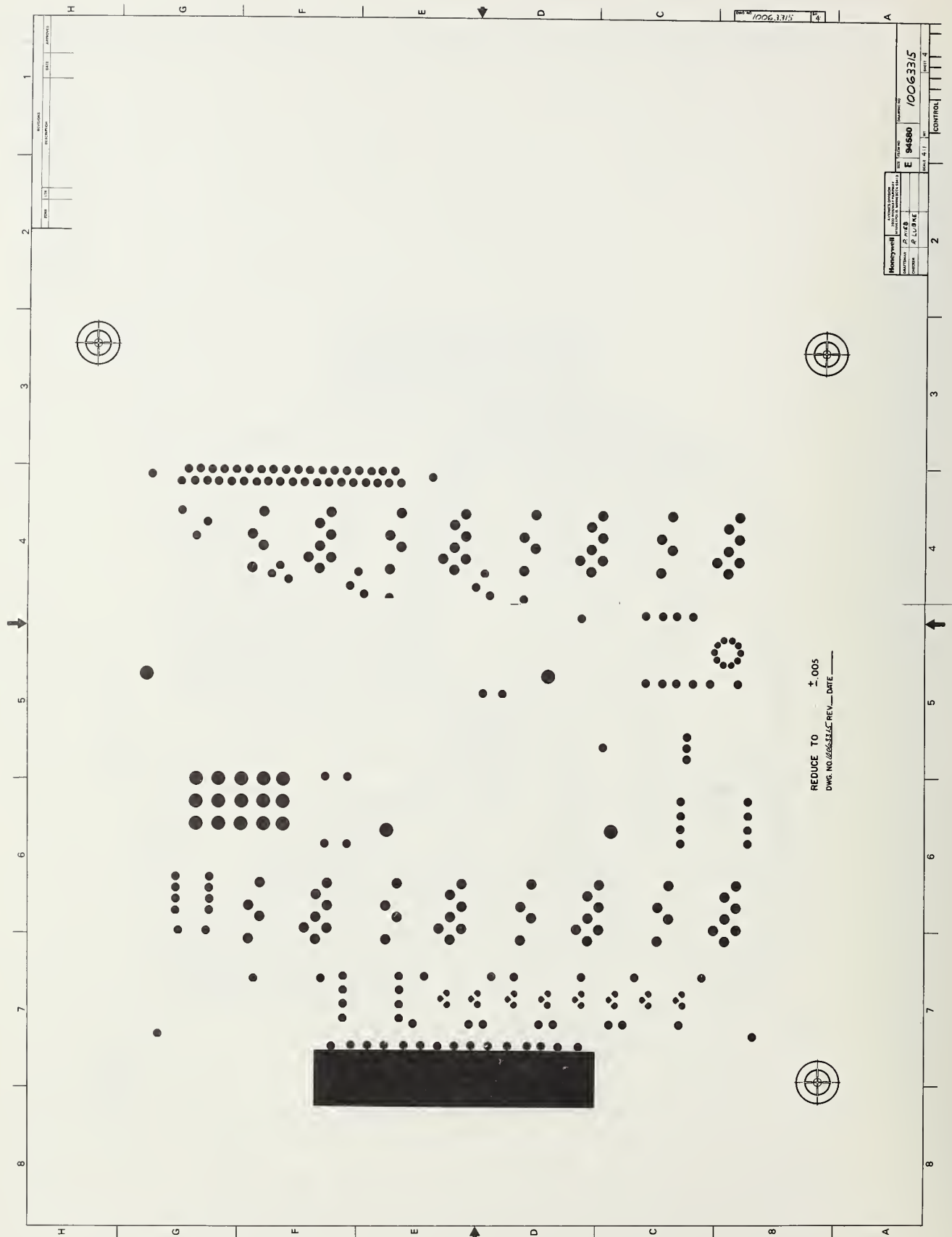




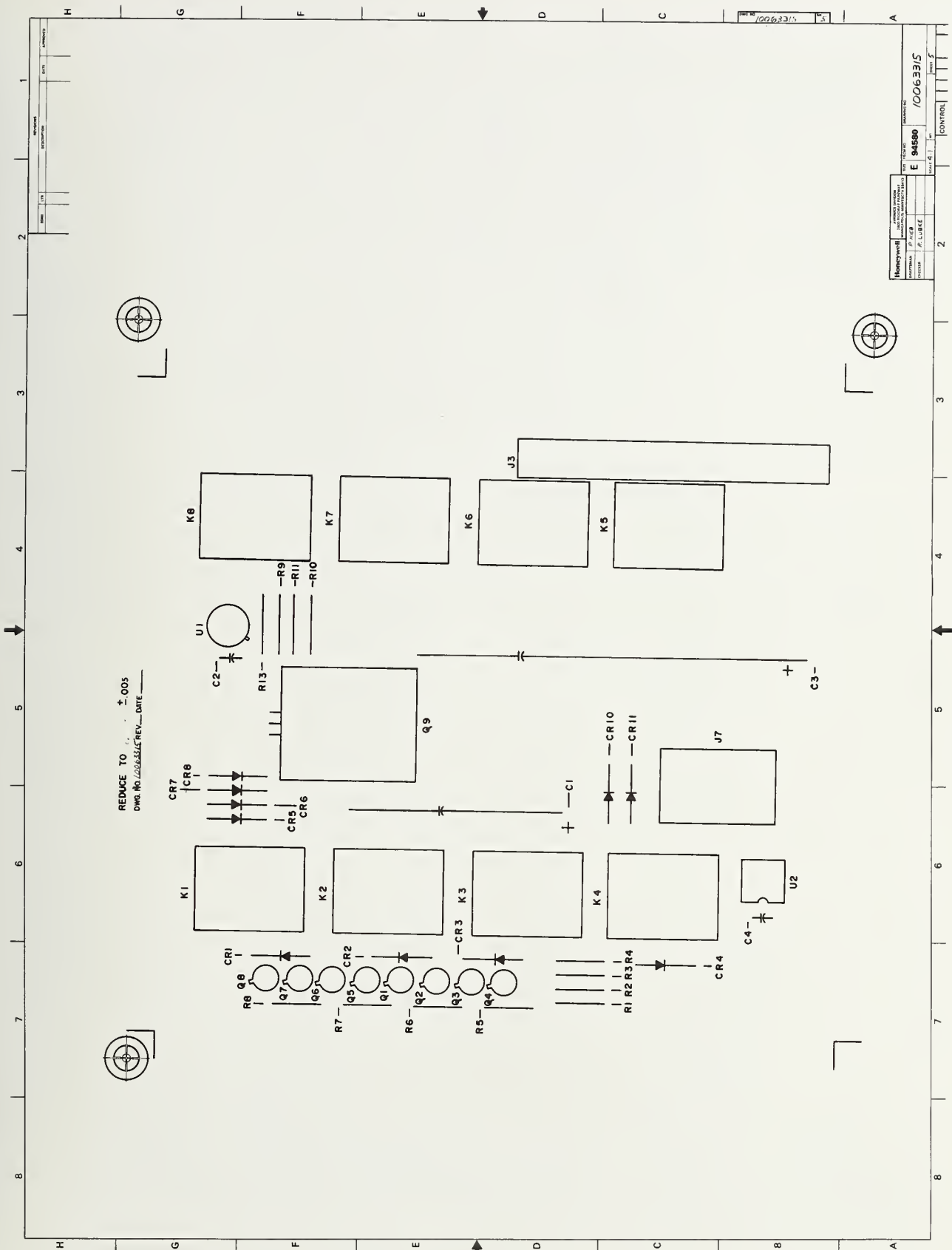








REDUCE TO  $\pm .005$   
 DWG NO. 10063315 REV. DATE









SUPERSEDES SUPERSEDED BY						ENGINEERING PARTS LIST				LOOPELECTRONICS		10059903	
REV.	DATE	E.O.	REV.	DATE	E.O.	TYPED BY	PPRD. BY	CHKD. BY	DATE	SHEETS	SHEET NO.		
A	10-10-77									3	1		
B	10-13-77												
PART NO.						PART NAME						QTY	
28021593-001						PANEL, FRONT						1	
T65F-02M						'F' POST BCD THUMBWHEEL						3	
T60						END CAP THUMBWHEEL SW						2	
7211A						SWITCH, TOGGLE						1	
OSL-3L						LED						3	
3009P-1-503						POTENTIOMETER 50K						1	
415-1230-01-18						HANDLE						2	
1-380949-2						RECEPTACLE ASSY						3	
MS3102						-14S-7P CONNECTOR						1	
CD4013						"D" FF						1	
CD4030						EXC OR						1	
CD4049						HEX INVERTER						1	
CA3100						OP AMP						1	
CA3130						OP AMP						1	
74C221						MONO MULTIVIBRATOR						1	
2N2222						TRANSISTOR						3	
1N5357						DIODE, ZENER, 20V						2	
200 KHZ						CRYSTAL						1	
RCR07G511JP						RESISTOR, 510						2	
RCR07G103JP						RESISTOR, 10K						4	
RCR07G153JP						RESISTOR, 15K						1	

Honeywell

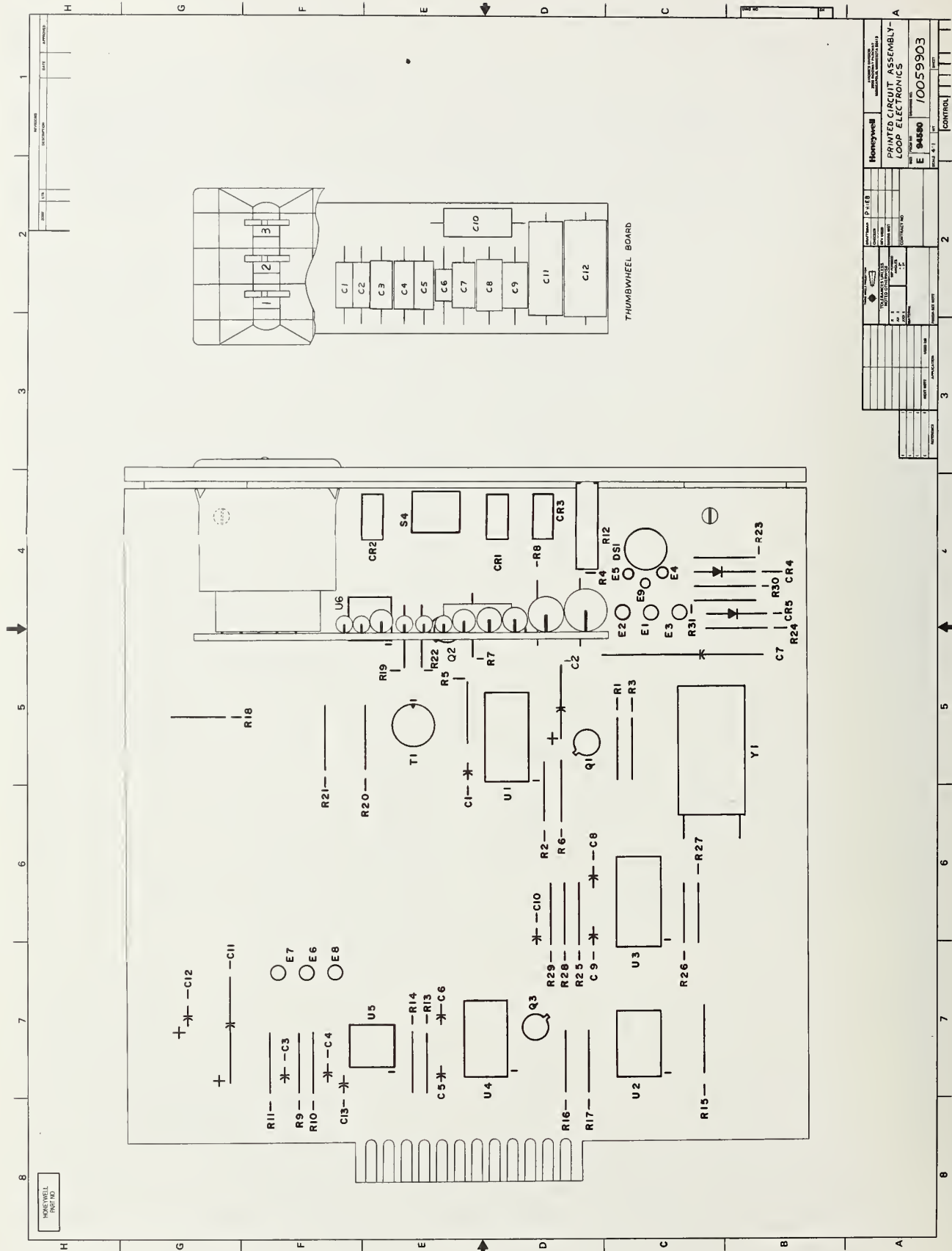
PRINTED IN U. S. A.

SUPERSEDES SUPERSEDED BY						ENGINEERING PARTS LIST				10059903	
REV.	DATE	E. O.	REV.	DATE	E. O.	LOOP ELECTRONICS				SHEETS	SHEET NO.
A	9-2-77					TYPED BY	PPRD. BY	CHKD. BY	DATE	3	2
PART NO. PART NAME						QTY					
RCR07G203JP RESISTOR, 20K						1	R17				
RCR07G273JP RESISTOR, 27K						2	R20, 21				
RCR07G333JP RESISTOR, 33K						1	R13				
RCR07G822JP RESISTOR, 8.2K						1	R29				
RCR07G104JP RESISTOR, 100K						3	R16, 23, 24				
RCR07G154JP RESISTOR, 150K						2	R27, 28				
RCR07G204JP RESISTOR, 200K						1	R10				
RCR07G334JP RESISTOR, 330K						1	R14				
RCR07G105JP RESISTOR, 1MEG						3	R5, 6, 9				
RCR07G512JP RESISTOR, 5.1K						2	R1, 2				
RW70U1001 RESISTOR, 1K						3	R4, 8, 15				
RT24C2P103 TRIMPOT, 10K						1	R18				
NE2 LAMP, NEON						1	DS1 (CR6)				
DIT270 TRANSFORMER						1	T1				UTC
8000-DG3 CRYSTAL HOLDER						1					AUGAT
CK05BX332K CAPACITOR .0033						1	C3				
TGS10 CAPACITOR .01						3	C6, 8, 12				DISC
CK05BX153K CAPACITOR .015						1	C4				
CK05BX104K CAPACITOR .1						3	C1, 9, 10				CERAMIC
CK06BX334K CAPACITOR .33						1	C5				
M39003/01-2365 CAPACITOR 3.3						1	C2				
M39003/01-2301 CAPACITOR 100						1	C11				20V
SX420 CAPACITOR 20pF						1	C1 POLYSTYRENE-MALLORY				
SX439 CAPACITOR 39pF						1	C2				

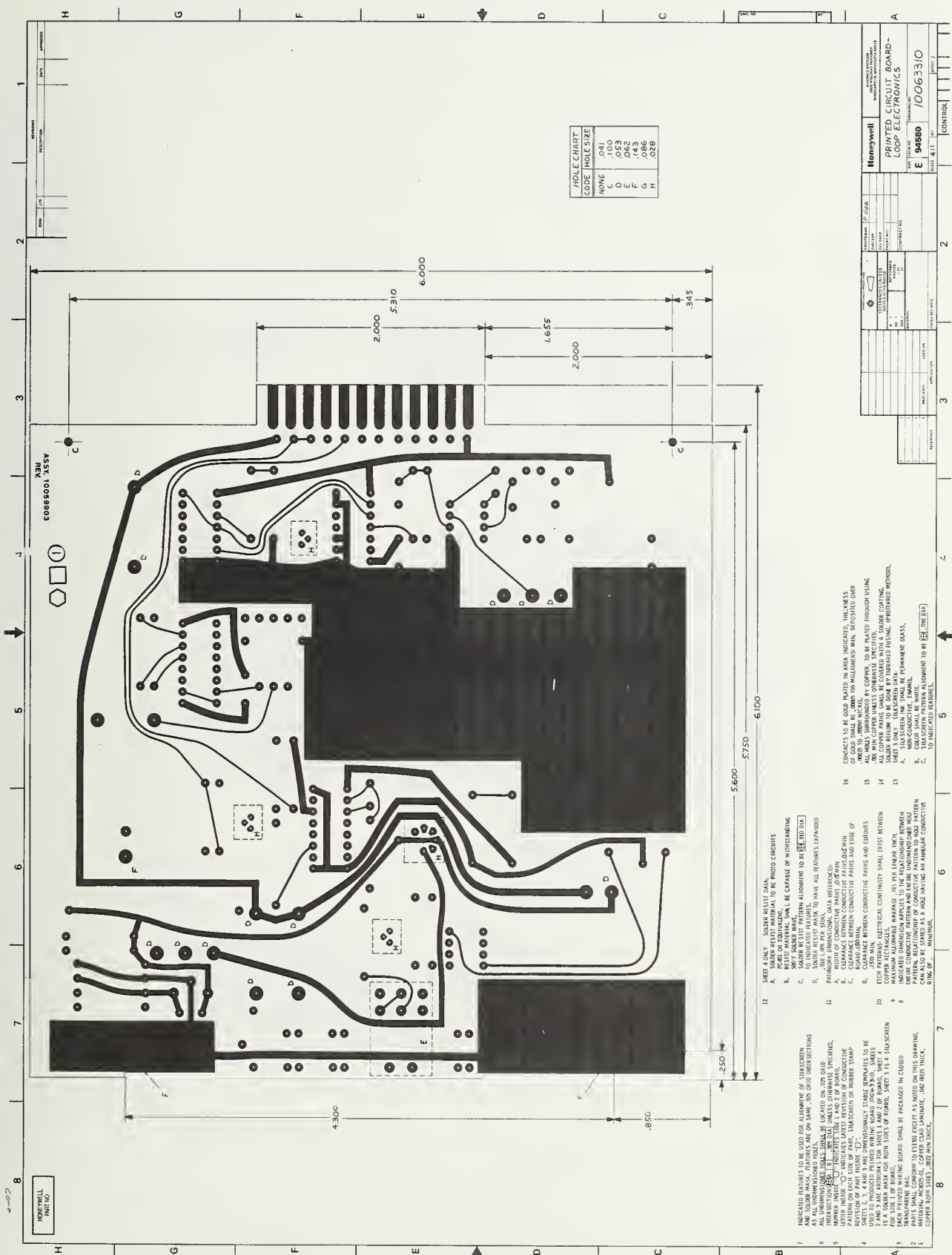
HE-124

PRINTED IN U. S. A.

HE-124







- 1 INDICATED FEATURES TO BE USED FOR ALIGNMENT OF SCREENS
- 2 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 3 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 4 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 5 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 6 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 7 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 8 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 9 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 10 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 11 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 12 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 13 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 14 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 15 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE
- 16 ALL UNDESIRABLE MATERIAL SHALL BE LOCATED ON ONE SIDE

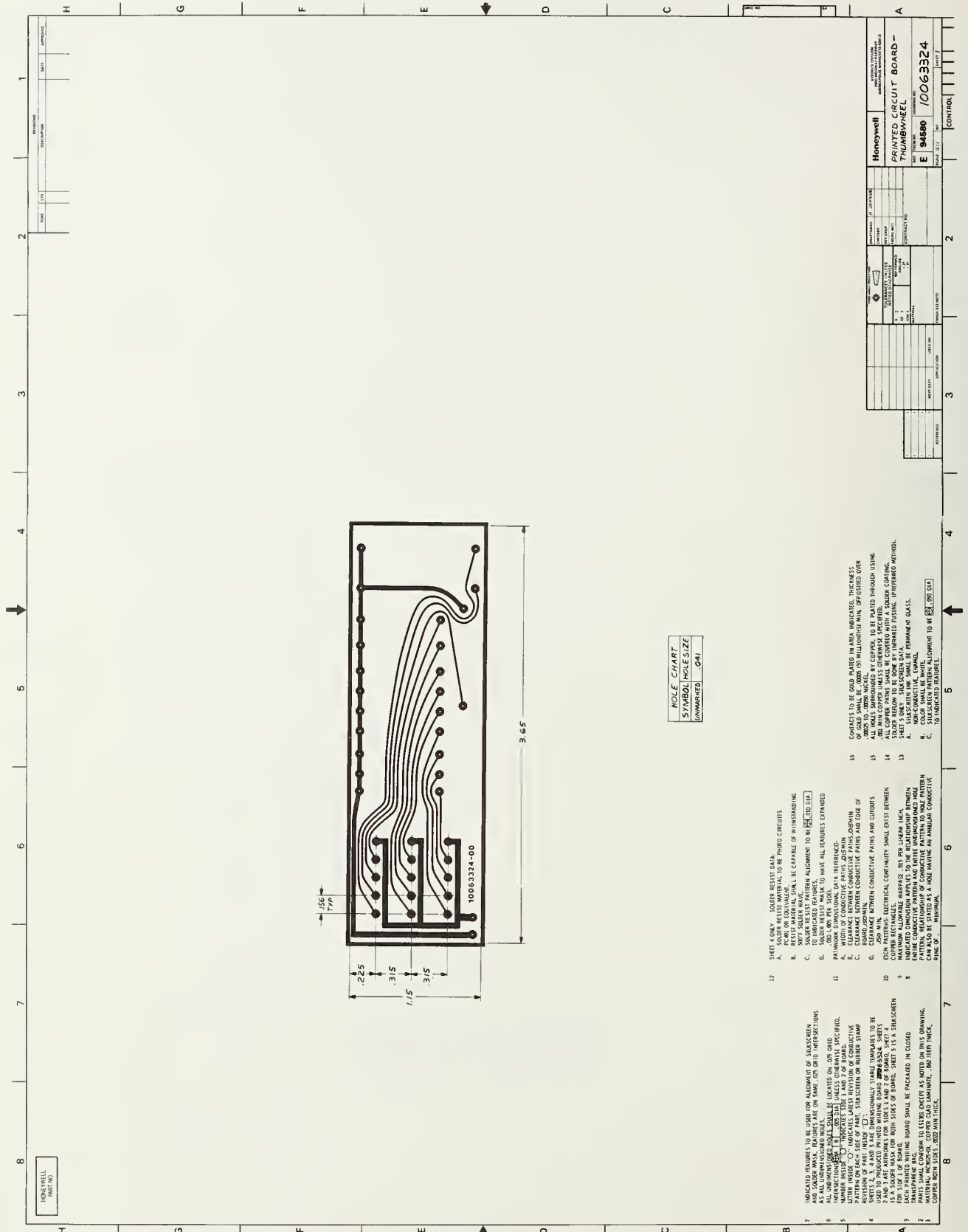


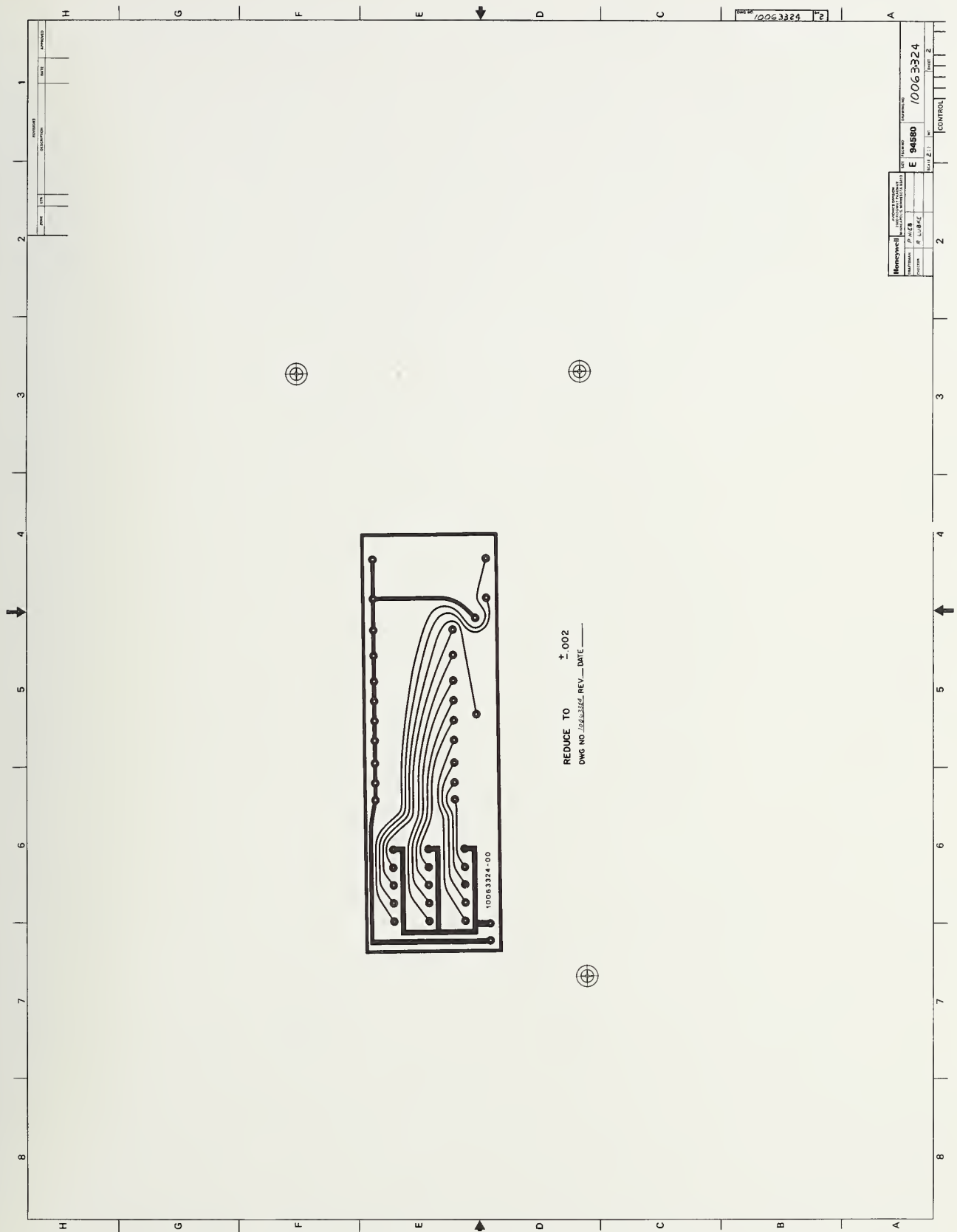






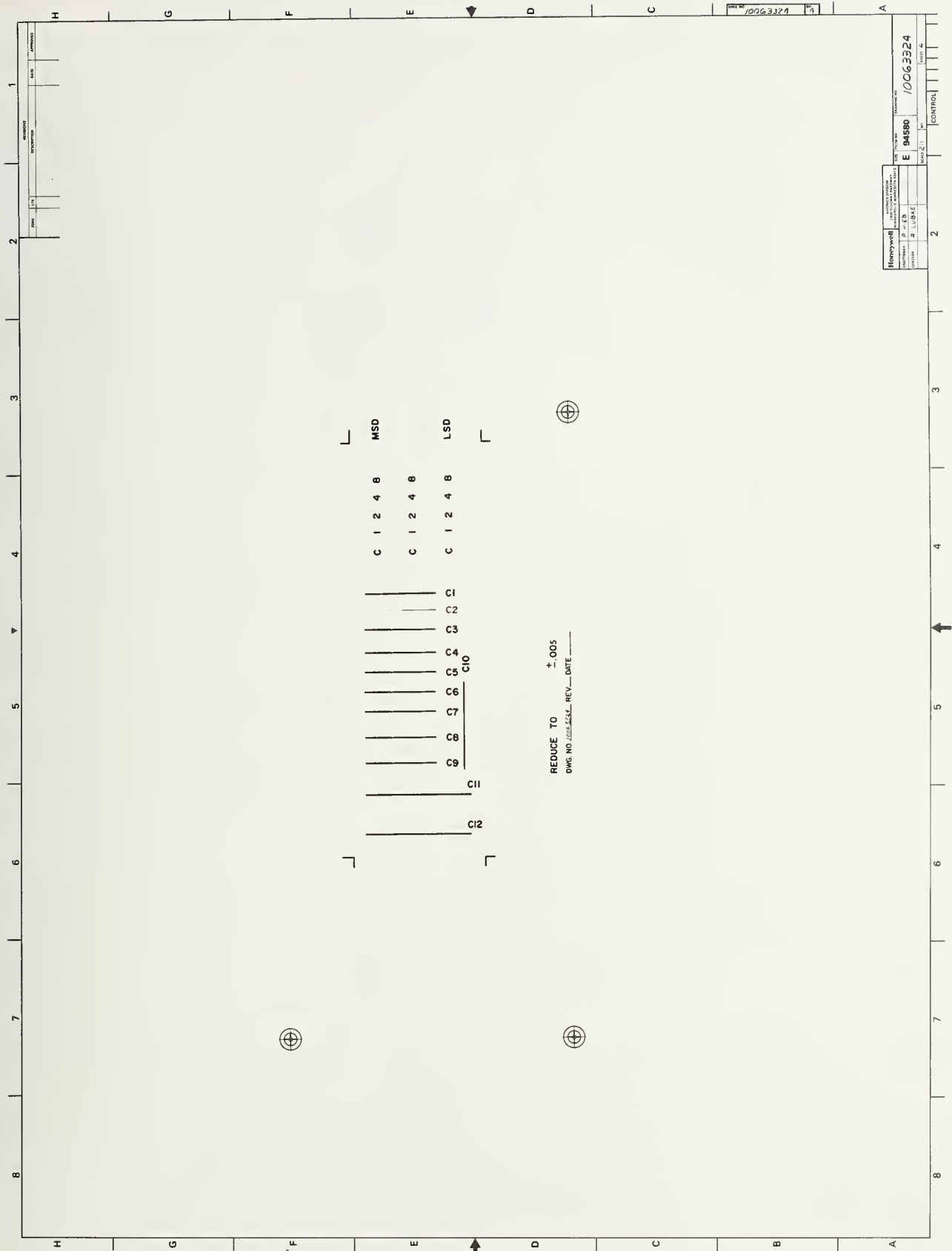










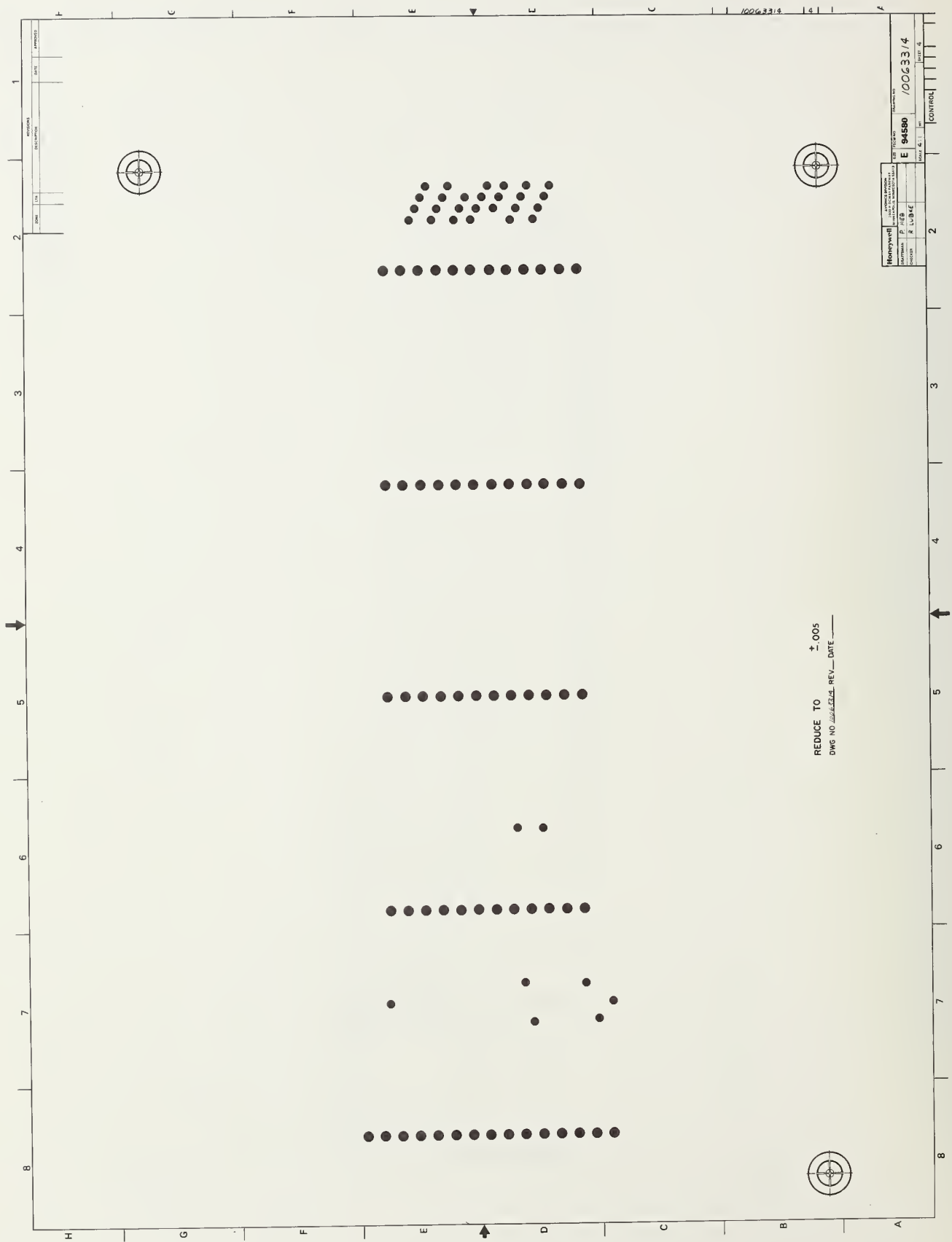












REDUCE TO  $\pm .005$   
 DWG NO 100633/4 REV. DATE

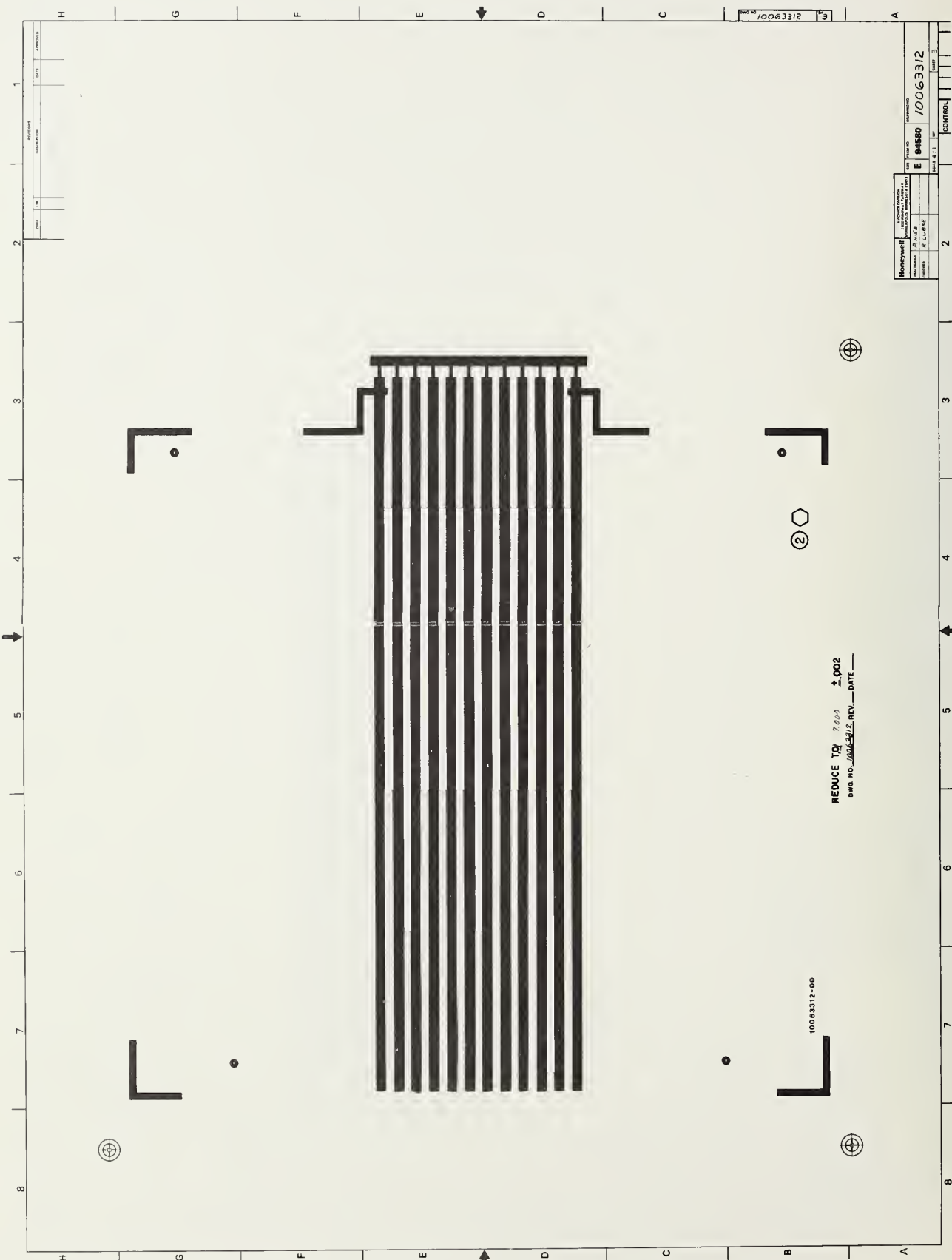
HONEYWELL 100633/4 100633/4	
DRAWN BY P. L. B.	CHECKED BY R. L. B.
DATE 10/1/68	REV. 1
CONTROL	

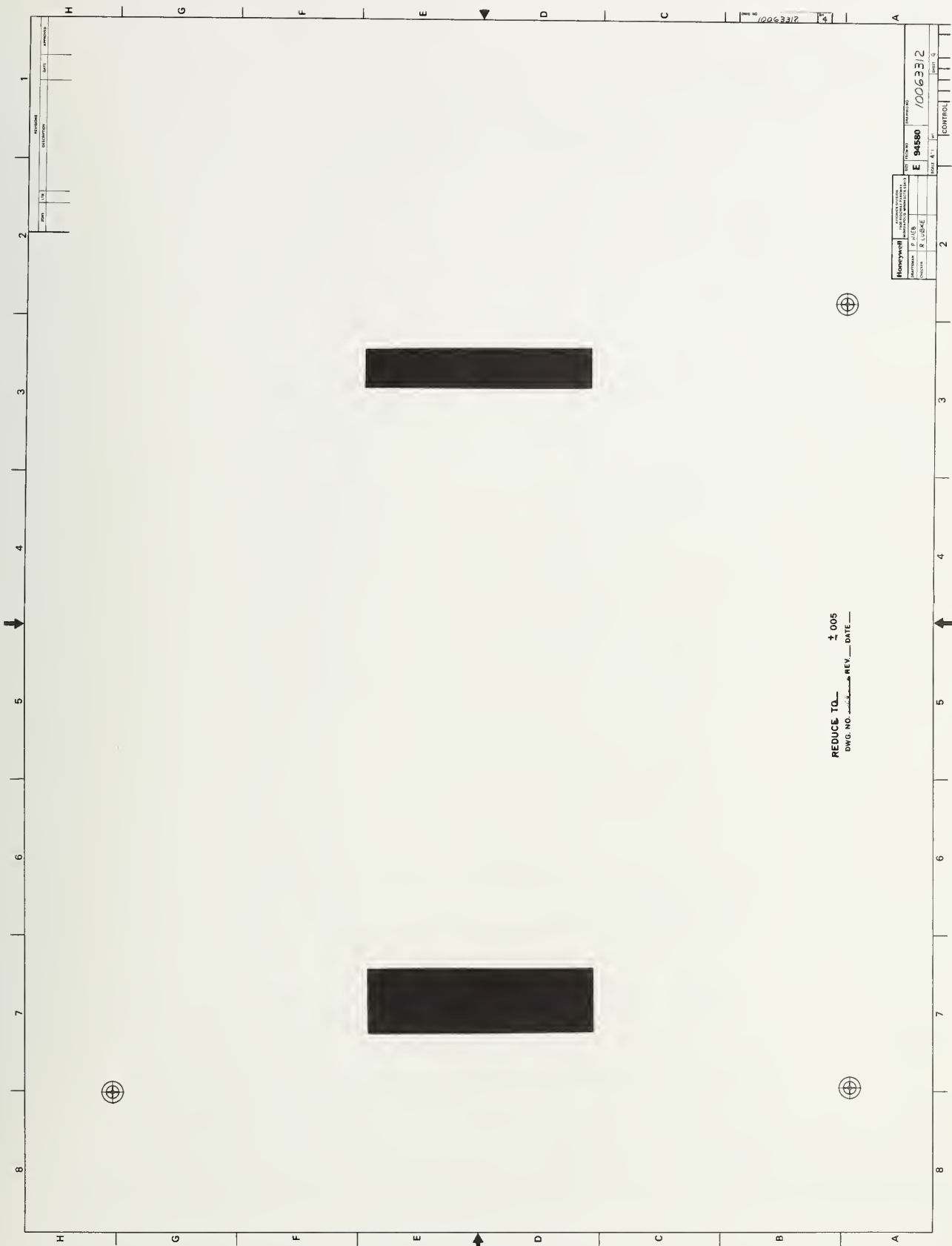












REDUCE TO 1/8" = 1'-0"  
 DWG. NO. 10063312 REV. DATE

REV.	DATE	BY	CHKD.	APP'D.
1				
2				
3				
4				
5				
6				
7				
8				

10063312	10063312
E 94580	
10063312	
10063312	





APPENDIX C  
PASSIVE BUS DETECTOR  
PREPROCESSOR PROGRAM LISTING

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
000	N00P	
1	BOC1, $243_{10}$	Go to preprocessor initialization if true.
2	ODSC, 3	Start A/D converter.
3	GN, CLRB	
4	TR, MEMU, A1	Read detector initialization flag.
5	AR, SUB	
6	JMPZ, $226_{10}$	Go to detector initialization.
7	TR, MEML, B	Read $b_i$
8	TR, DIR, A1	Read $k_n$
9	AR, SUB	$k_n - b_i$
010	TR, A0, C	Save $k_n - b_i$
1	JMPL, $206_0$	
2	TR, A0, A1	
3	TR, T, B	Read T
4	AR, SUB	$k_n - b_i - T$
5	JMPL, $142_{10}$	
6	GN, IMAR	
7	TR, MEMU, A1	Read presence flag.
8	BOC4, $026_{10}$	Resence flag set.
9	AR, A1 + 1	A1 = 0.
020	TR, A0, MEMU	Set presence flag.
1	GN, IMAR	
2	TR, A0, MEM	Set internal time to 1.
3	GN, IMAR	
4	TR, A0, MEMU	Set positive slope flag.

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
025	JMPU, $041_{10}$	
6	TR, MEM, MMDR	Transfer presence flag word to data register.
7	GN, IMAR	
8	TR, MEM, A1	Read cumulative time interval (CTI).
9	AR, $A1 + 1$	
030	BOC3, $032_{10}$	Overflow?
1	TR, A0, MEM	Store CTI.
2	CMB, $11_{10}$	
3	AR, SUB	CTI - 11.
4	JMPL, 040	
5	TR, MAR, A1	Read MAR at CTI.
6	CMB, $5_{10}$	
7	AR, ADD	Locate CTI + 5.
8	TR, A0, MMAR	
9	ODSC, 6	Set vehicle presence in IMP-16C.
040	GN, IMAR	
1	GN, IMAR	
2	TR, C, A1	Recall $k_n - b_i$
3	TR, MEM, B	Read $k_{n-1}$
4	AR, SUB	$(k_n - b_i) - k_{n-1}$
5	JMPO, $114_{10}$	
6	JMPG, $114_{10}$	Positive slope?
7	GN, DMAR	
8	TR, MEMU, A1	Read slop flag.
9	BOC4, $051_{10}$	Flag set?

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
050	JMPU, 130 <sub>10</sub>	
1	GN, IMAR	
2	TR, MEM, A1	Read $k_{n-1}$
3	TR, C, B	Recall $k_n - b_i$
4	AR, SUB	$k_{n-1} - (k_n - b_i)$
5	JMPL, 132 <sub>10</sub>	
6	TR, A0, A1	
7	TR, Epsilon, B	Read epsilon-switch
8	AR, SUB	$k_{n-1} - (k_n - b_i) - \text{epsilon}$
9	JMPL, 132 <sub>10</sub>	
060	TR, MEM, MMDR	Save peak value.
1	TR, C, MEM	Store $k_n - b_i$ on $k_{n-1}$
2	GN, IMAR	
3	TR, MEMU, A1	Read number of peaks.
4	CMB, 3	
5	AR, SUB	Number of peaks - 3.
6	JMPO, 074 <sub>10</sub>	= 0?
7	JMPG, 074 <sub>10</sub>	> 0?
8	AR, A1 + 1	
9	TR, A0, MEMU	Store number of peaks.
070	TR, MEML, A1	Read adx index.
1	AR, A1 + 1	
2	TR, A0, MEML	Store adx index.
3	JMPU, 077 <sub>10</sub>	
4	TR, MEML, A1	Read adx index.
5	AR, A1 - 1	
6	TR, A0, MEML	Store adx index.
7	TR, MAR, A1	Read MAR.
8	CMB, 370 <sub>8</sub>	
9	AR, AND	Mask.

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
080	TR, A0, B	Detector base adx.
1	TR, MEML, A1	Read adx index.
2	AR, ADD	Make peak value adx.
3	TR, A0, MMAR	
4	ODSC, 6	Store peak value in IMP-16C.
5	AR, A1 + 1	
6	TR, A0, MEML	Update adx index.
7	TR, A0, A1	
8	AR, ADD	Make internal adx.
9	TR, MAR, C	Save MAR = adx index.
090	GN, DMAR	
1	GN, DMAR	
2	TR, A0, MMAR	Load internal adx.
3	TR, C, A0	Save C.
4	GN, CLRC	
5	TR, C, MEMU	Clear slope flag.
6	GN, DMAR	
7	TR, MEM, MMDR	Read cumulative interval.
8	ODSC, 6	Store CTI.
9	N00P	
100	TR, A0, MAR	Restore MAR.
1	TR, MEMU, A1	Read number of peaks.
2	CMB, 1	
3	AR, SUB	Number of peaks - 1.
4	JMPG, 132 <sub>10</sub>	
5	TR, C, MMDR	(C) = 0.
6	TR, MAR, MMAR	Last amplitude data adx.
7	ODSC, 6	Clear last amplitude data.
8	GN, IMAR	
9	GN, IMAR	

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
110	TR, MAR, MMAR	Load ESS adx.
1	ODSC, 6	Clear ESS.
2	JMPU, 132 <sub>10</sub>	
3	GN, HALT	Should not be executed.
4	GN, DMAR	
5	TR, MEMU, A1	Read slope flag.
6	BOC4, 130 <sub>10</sub>	Slope flag set?
7	GN, IMAR	
8	TR, C, A1	Recall $k_n - b_i$
9	TR, MEM, B	Read $k_{n-1}$
120	AR, SUB	$(k_n - b_i) - k_{n-1}$
1	TR, A0, A1	
2	TR, Epsilon, B	Read epsilon-switch
3	AR, SUB	$(k_n - b_i) - k_{n-1} - \text{epsilon}$
4	JMPL, 132 <sub>10</sub>	
5	N00P	
6	GN, DMAR	
7	TR, MEMU, A1	Read slope flag.
8	AR, A1 + 1	
9	TR, A0, MEMU	Set slope flag.
130	GN, IMAR	
1	TR, C, MEM	Store $k_n - b_i$ in $k_{n-1}$
2	TR, MAR, A1	
3	CMB, 370 <sub>8</sub>	
4	AR, AND	Mask.
5	TR, A0, A1	
6	CMB, 8	
7	AR, ADD	Make new detector adx.
8	TR, A0, MAR	
9	N00P	

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
140	JMPU, 139 <sub>10</sub>	Wait loop.
1	N00P	From 011.
2	GN, IMAR	From 015.
3	TR, MEMU, A1	Read presence flag.
4	BOC4, 146 <sub>10</sub>	
5	JMPU, 205 <sub>10</sub>	Go to long-term signal average.
6	TR, C, A1	Recall $k_n - b_i$ .
7	AR, A1 + 1	
8	TR, A0, A1	
9	TR, T, B	Read T-switch.
150	AR, SUB	$(k_n - b_i) + 1 - T$ .
1	JMPG, 185 <sub>10</sub>	
2	TR, MEMU, A1	Read presence flag.
3	AR, A1 - 1	
4	TR, A0, MEMU	Reset presence flag.
5	GN, DMAR	
6	TR, MAR, C	Save MAR.
7	GN, IMAR	
8	GN, IMAR	
9	TR, MEM, A1	Read CTI.
160	CMB, 10 <sub>10</sub>	
1	AR, SUB	CTI-10.
2	JMPL, 177 <sub>10</sub>	
3	AR, A1 + 1	Increment CTI.
4	BOC3, 167 <sub>10</sub>	Overflow?
5	TR, A0, MMDR	
6	JMPU, 168 <sub>10</sub>	
7	TR, MEM, MMDR	
8	TR, C, MMAR	
9	0DSC, 6	Store lost interval time.



<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
170	TR, C, A1	Recall MAR.
1	CMB, 7	
2	AR, ADD	Make status bit adx.
3	TR, A0, MMAR	
4	CMC, 1	
5	TR, C, MMDR	
6	0DSC, 6	Set ESS and clear VEH status.
7	GN, CLRC	
8	TR, C, MEM	Clear CTI.
9	GN, IMAR	
180	GN, IMAR	
1	TR, C, MEM	Clear $k_{n-1}$ .
2	GN, IMAR	
3	TR, C, MEM	Clear number of peaks and adx index.
4	JMPU, 132 <sub>10</sub>	
5	GN, IMAR	From 151.
6	TR, MEM, A1	Read CTI.
7	AR, A1 + 1	
8	BOC3, 132 <sub>10</sub>	Overflow?
9	TR, A0, MEM	Store CTI.
190	JMPU, 132 <sub>10</sub>	Go to detector adx update.
1	N00P	
2	N00P	
3	N00P	
4	N00P	
5	N00P	
6	<b>N00P</b>	
7	N00P	
8	N00P	
9	N00P	

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
200	GN, CLRC	Used for debug only.
1	TR, C, MAR	Used for debug only.
2	GN, IMAR	Used for debug only.
3	JMPU, 202	Used for debug only.
4	N00P	
5	GN, DMAR	Extry from FEX at 145 <sub>10</sub> .
6	TR, MAR, C	Save MAR; Entry from 011.
7	TR, MAR, A1	Make update timer adx.
8	CMB, 6	Make update timer adx.
9	AR, ADD	Make update timer adx.
210	TR, A0, Mar	Make update timer adx.
1	TR, MEM, A1	Read update interval
2	CMB, 255 <sub>10</sub>	
3	AR, SUB	Timer - 256
4	JMPL, 221 <sub>10</sub> <sup>BB</sup>	Is interval > 0.97 sec?
5	TR, A0, A1	
6	CMB, 255 <sub>10</sub>	(Timer - 256) - 256.
7	AR, SUB	
8	JMPL, 220AA	Is interval ≥ 1.95 sec?
9	JMP0, 224CC	Is interval ≥ 1.95 sec?
220	TR, MEM, A1	Read update interval
1	AR, A1 + 1	
2	TR, A0, MEM	Store update interval.
3	JMPU, 132 <sub>10</sub>	Go to detector update.
4	TR, A0, MEM	Clear update interval
5	TR, C, MAR	Restore MAR.
6	TR, DIR, B	Read k <sub>n</sub> ; Enry to detector initial- ization from 006.
7	TR, MEML, A1	Read b <sub>i</sub> .
8	AR, SUB	b <sub>i</sub> - k <sub>n</sub> .
9	JMPO, 236DD	

<u>Step</u>	<u>Signal</u>	<u>Instruction</u>
230	JMPL, 233	Is bias < $k_n$ ?
1	AR, A1 - 1	Decrement $b_i$ .
2	JMPU, 234	
3	AR, A1 + 1	Increment $b_i$ .
4	TR, A0, MEML	Store $B_i$ .
5	JMPU, 241	
6	TR, MEMU, A1	
7	BOCr, 241 <sub>10</sub>	
8	N00P	Read detector initialization flag.
9	AR, A1 + 1	
240	TR, A0, MEMU	Set initialization flag.
1	JMPU, 132 <sub>10</sub>	Go to detector update.
2	GN, HALT	
3	GN, CLRC	
4	TR, C, MAR	
5	TR, C, A1	
6	TR, C, MEM	
7	AR, A1 + 1	
8	BOC3, 252 <sub>10</sub>	
9	TR, A0, A1	
250	GN, IMAR	
1	JMPU, 246 <sub>10</sub>	
2	0DSC, 1	
3	TR, C, MAR	
4	N00P	
255	JMPU, 254 <sub>10</sub>	



# APPENDIX D

## IMP-16C PROGRAM LISTING

SNUMB = PB0U XX  
 XXX

XXXXX	XXXX	XXXXX	X	X
X X	X X	X X	X	X
XXXXX	XXXXX	X X	X	X
X	X X	X X	X	X
X	X X	X X	X	X
X	XXXXX	XXXXX	XXXX	

XX  
 XXX

\$\$ PB0U ENTERED CS-H.0 AT 09.173 FROM SYSTEM-0 REMOTE 0-08-03

0001 \$	SNUMB	PB0U	
0002 \$	IOENT	G10627	
0003 \$\$	USERIO	G10627\$###	
0004 \$	OPTIONS	FORTRAN,NOMAP	
0005 \$\$	SELECT	G02771/NATIONAL/POINTER	
0006* \$\$	SELECT	G02771/NATIONAL/ASMIMP16	
0007* \$	OBJECT		Y10.768070275BINSCH00
0008* \$	DKENO	CONTINUE	BINSCH07
0009* \$	OBJECT		Y10.769070275STRING00
0010* \$	DKENO	CONTINUE	STRING06
0011* \$	OBJECT		Y10.769070275LABEL000
0012* \$	OKEND	CONTINUE	LABEL006
0013* \$	OBJECT		Y10.770070275LCVAL000
0014* \$	DKENO	CONTINUE	LCVAL004
0015* \$	OBJECT		Y10.770070275I2HEX000
0016* \$	DKENO	CONTINUE	I2HEX006
0017* \$	OBJECT		Y10.771070275DEC21000
0018* \$	DKENO	CONTINUE	DEC21007
0019* \$	OBJECT		Y10.771070275UNPACK00
0020* \$	DKENO	CONTINUE	UNPACK06
0021* \$	OBJECT		Y10.772070275SYMBOL00
0022* \$	DKENO	CONTINUE	SYMBOL11
0023* \$	OBJECT		Y10.772070275HEX21000
0024* \$	OKEND	CONTINUE	HEX21007
0025* \$	OBJECT		Y10.773070275ASC21000
0026* \$	DKENO	CONTINUE	ASC21007
0027* \$	OBJECT		Y10.773070275FORM0000
0028* \$	DKENO	CONTINUE	FORM0015
0029* \$	OBJECT		Y10.773070275NXCHAR00
0030* \$	OKEND	CONTINUE	NXCHAR14
0031* \$	OBJECT		Y10.774070275PSECT000
0032* \$	DKEND	CONTINUE	PSECT003
0033* \$	OBJECT		Y10.774070275REMOVE00
0034* \$	DKEND	CONTINUE	REMOVE05
0035* \$	OBJECT		Y10.775070275OR000000
0036* \$	OKEND	CONTINUE	OR000009
0037* \$	OBJECT		Y10.775070275AN000000
0038* \$	DKEND	CONTINUE	AN000009
0039* \$	OBJECT		Y10.775070275INSERT00
0040* \$	OKEND	CONTINUE	INSERT06
0041* \$	OBJECT		Y10.776070275ERRCOL00
0042* \$	OKEND	CONTINUE	ERRCOL04
0043* \$	OBJECT		Y10.776070275EVAL0000
0044* \$	DKEND	CONTINUE	EVAL0020
0045* \$	OBJECT		Y10.777070275DATA0000

0046* \$	DKEND	CONTINUE	DATA0009
0047* \$	OBJECT		Y10.777070275ASSIGN00
0048* \$	DKEND	CONTINUE	ASSIGN06
0049* \$	OBJECT		Y10.777070275PRFORM00
0050* \$	DKEND	CONTINUE	PRFORM12
0051* \$	OBJECT		Y10.778070275LCNTL000
0052* \$	DKEND	CONTINUE	LCNTL009
0053* \$	OBJECT		Y10.778070275MEMREF00
0054* \$	DKEND	CONTINUE	MEMREF26
0055* \$	OBJECT		Y10.778070275MISCIN00
0056* \$	DKEND	CONTINUE	MISCIN10
0057* \$	OBJECT		Y10.779070275LCMOD000
0058* \$	DKEND	CONTINUE	LCMOD006
0059* \$	OBJECT		Y10.779070275XMTREC00
0060* \$	DKEND	CONTINUE	XMTREC06
0061* \$	OBJECT		Y10.779070275NXPAGE00
0062* \$	DKEND	CONTINUE	NXPAGE09
0063* \$	OBJECT		Y10.780070275NXITEM00
0064* \$	DKEND	CONTINUE	NXITEM08
0065* \$	OBJECT		Y10.780070275.....00
0066* \$	DKEND	CONTINUE	.....11
0067* \$	OBJECT		Y10.780070275ACNTL000
0068* \$	DKEND	CONTINUE	ACNTL014
0069* \$	OBJECT		Y10.781070275LIST0000
0070* \$	DKEND	CONTINUE	LIST0029
0071* \$	OBJECT		Y10.781070275REGINT00
0072* \$	DKEND	CONTINUE	REGINT12
0073* \$	OBJECT		Y10.782070275INST0000
0074* \$	DKEND	CONTINUE	INST0032
0075* \$	OBJECT		Y10.78207027500000000
0076* \$	DKEND	CONTINUE	00000014
0077* \$	OBJECT		Y10.782070275SYMVAl00
0078* \$	DKEND	CONTINUE	SYMVAl10
0079* \$	OBJECT		Y10.783070275EXTSYM00
0080* \$	DKEND	CONTINUE	EXTSYM05
0081* \$	OBJECT		Y10.783070275NXTSYM00
0082* \$	DKEND	CONTINUE	NXTSYM07
0083* \$	OBJECT		Y10.783070275ADDSYM00
0084* \$	DKEND	CONTINUE	ADDSYM21
0085* \$	OBJECT		Y10.784070275ADPART00
0086* \$	DKEND	CONTINUE	ADPART21
0087* \$	OBJECT		Y10.784070275ERREPT00
0088* \$	DKEND	CONTINUE	ERREPT23
0089* \$	OBJECT		Y10.784070275DIRECT00
0090* \$	DKEND	CONTINUE	DIRECT14
0091* \$	OBJECT		Y10.785070275BOCNTL00
0092* \$	DKEND	CONTINUE	BOCNTL12
0093* \$	OBJECT		Y10.785070275GENRLM00
0094* \$	DKEND		GENRLM25
0095 A\$	EXECUTE		
0096 \$	LIMITS	15,23K,.,7500	
0097 \$\$	PRMFL	09,R/W,S,G10627/IMPOBJC	
0098 \$	SET	6,19	
0099 \$	FILE	10,X1S,40L	
0100 \$	DATA	05	
0101 \$\$	SELECT	G10627/CONSTANT	
0102 \$\$	SELECT	G10627/BASEPG	
0103 \$\$	SELECT	G10627/XEC	
0104 \$\$	SELECT	G10627/VCLAS	
0105 \$\$	SELECT	G10627/BAKGRND	
0106 \$\$	SELECT	G10627/DATABSE	
0107 \$	INCODE	IBMEL	
0108 \$	IF	/19,ENDJOB	
0109 \$	OPTIONS	FORTRAN,NOMAP	
0110 \$	LIBRARY	L1	
0111 \$\$	SELECT	G02771/NATIONAL/XREF	



```

0112* $      OBJECT                                Y16.706071475.....00
0113* $      DKEND                                  .....21
0114 AS     EXECUTE
0115 $      LIMITS  +20K
0116 $$     PRMFL  L1,R,R,USERLIB/UTILITY/BUTIL
0117 $      FILE   10,X1R
0118 $      FILE   11,X2R,40L
0119 $      FILE   S1,X3R,44R
0120 $      ENDJOB
TOTAL CARD COUNT THIS JDB = 002501

```

```

* ACTY-01 $CARD #0095 GELDAD 08/30/77 SW=014000200000
* NDRMAL TERMINATION AT 013463 I=5020 SW=014000200000

```

START	9.185	LINES	2209	PRDC	0.0174	I/O	0.003	IU	5	MEMORY	23K
STDP	9.215	LIMIT	7500	LIMIT	0.1500	LIMIT		CU	5	M*T	2737
SWAP	0.000										
LAPSE	0.030	FC D	TYPE	BUSY	IP/AT	FP/RT	IS/#C	MS/#E	ADDRESS	T#/PK#	
		05 R	D450 *	4004	0	91	91	91	0-08-03		
		R* R	D450 *	1012	0	0	46	46	0-08-03		
		09 R	D450 P	132	0	6	13	13	0-08-07		
		10 S	D450 *	616	0	0	480	480	0-08-08		
		P*	SYDUT								
		L* R	D450 *	1540	0	0	800	800R	0-08-05		
		*L R	D450 *	44	0	0	170	170R	0-08-05		

```

LIST 18 LINES AT STA. G5
RC-06 2191 LINES AT STA. G5

```

```

ACTIVITY 01 COST=$ 8.21
*CUMULATIVE COST=$ 8.21

```

```

* ACTY-02 $CARD #0114 GELDAD 08/30/77 SW=000000200000
SORT ENGAGED - VERSION: 3-CB/1

```

```

FILE 11 UNSUITABLE FOR COLLATION.
MEMORY: 023416 LINKS: 00044 INPUT: 0320/DDUBLE OUTPUT: 0320/DDUBLE COLLATION: 0330/DDUBLE TDURNAMENT: 000493 ENTRIES
END OF FILE ON 10. RECORDS READ = 00002147. RECORDS ACCEPTED = 00002147. RECORDS DELETED = 00000000.
MERGING 000003 STRINGS 04 WAYS.
LINK UTILIZATION. ALLOCATED 00044 BDRRDWED 00000 USED 00003
RECORDS INPUT = 00002147. RECORDS OUTPUT = 00002147.

```

```

SORT TERMINATES.

```

```

* NORMAL TERMINATION AT 013263 I=5020 SW=000000200000

```

START	9.220	LINES	767	PRDC	0.0014	I/D	0.002	IU	5	MEMORY	20K
STDP	9.239	LIMIT	5000	LIMIT	0.0500	LIMIT		CU	5	M*T	775
SWAP	0.009										
LAPSE	0.018	FC D	TYPE	BUSY	IP/AT	FP/RT	IS/#C	MS/#E	ADDRESS	T#/PK#	
		10 R	D450 *	638	0	0	480	480	0-08-08		
		P* R	D450 *	66	0	0	3	3	0-08-03		
		L1 R	D450 P	88	0	0	120	120R	0-08-02		
		11 R	D450 *	1386	0	28	480	480	0-08-03		
		S1 R	D450 *	1188	0	0	528	528R	0-08-03		
		P*	SYDUT								
		L* R	D450 *	1584	0	0	800	800R	0-08-05		
		*L R	D450 *	44	0	0	170	170R	0-08-05		

```

LIST 21 LINES AT STA. G5
RC-06 746 LINES AT STA. G5

```

```

ACTIVITY 02 COST=$ 0.78

```

```

*CUMULATIVE COST=$ 8.99

```

```

SNUMB = PBDU , ACTIVITY # = 01 , , REPORT CODE = 74 , RECORD COUNT = 000018

```

ORIGIN DATE MODULE ENTRY LOCATION ENTRY LOCATION ENTRY LOCATION ENTRY LOCATION ENTRY LOCATION

SUBPROGRAMS INCLUDED IN DECK.

\$ OPTIONS FDPTRAN,NOMAP

SUBPRDGRAMS OBTAINED FROM SYSTEM LIBRARY

	RANGE	SIZE
ALLOCATED CDRE	000000 THRU 055777	056000
RELOCATABLE	004054 THRU 055777	051724
\$ PRMFL	09,R/W,S,G10627/IMPDBJC	
\$ FILE	10,X15,40L	
\$ DATA	05	

FCB AND BUFFER SPACE		
AVAILABLE	000101 THRU 004053	003753
FILE CTRL BLKS	003622 THRU 004054	000233
MAXIMUM BUFFER SPACE REQUIRED		003105

23K. IS THE MINIMUM MEMORY NEEDED TO LOAD THIS ACTIVITY WITH ALL FILES OPEN 740808 2/H  
001456 LOCATIONS REQUIRED FOR LOAD TABLE  
EXECUTION PROGRAM ENTERED AT 033506 THROUGH .FSETU

SNUMB = PBDU , ACTIVITY # = 01, , REPORT CODE = 06, RECORD COUNT = 002191

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PBDU PRODUCTION PROTOTYPE

08/30/77 9.187  
PAGE NUMBER 1

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PBDU PRODUCTION PROTOTYPE

08/30/77 9.187  
PAGE NUMBER 2

```

3 0000      ;      .LIST 1
4 0000      ;
5 0000      ;
6 0000      ;
7 0000      ;      *****
8 0000      ;      *****
9 0000      ;
10 0000     ;
11 0000     ;
12 0000     ;      PASSIVE BUS DETECTOR UNIT
13 0000     ;
14 0000     ;
15 0000     ;
16 0000     ;      *****
17 0000     ;      *****
18 0000     ;
19 0000     ;
20 0000     ;
21 0000     ;      MEMORY MAPPED AS FOLLOWS:
22 0000     ;
23 0000     ;      0000-00FF : BASE PAGE PROM
24 0000     ;      1000-17FF : PBDU PROGRAM PROM
25 0000     ;      3000-32FF : DATA BASE RAM
26 0000     ;      3300-33FF : CCU (DANYL) RAM
27 0000     ;      EF00-EFFF : CCU PROGRAM PROM
28 0000     ;      FF00-FFFF : TOP PAGE PROM
    
```

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 PBDU PRODUCTION PROTOTYPE  
 ASSEMBLY CONSTANTS

08/30/77 9.187  
 PAGE NUMBER 3

```

32 0000          .LIST   LAC
33 0000          ;
34 0000          ;
35 0000          ;
36 0000          ;
37 0000 0000 A AC0   =      0          ; ACCUMULATOR 0
38 0000 0001 A AC1   =      1          ; ACCUMULATOR 1
39 0000 0002 A AC2   =      2          ; ACCUMULATOR 2
40 0000 0003 A AC3   =      3          ; ACCUMULATOR 3
41 0000          ;
42 0000 0000 A FC0   =      X'0        ; WRITE BUS DETECTED WORD
43 0000 0001 A FC1   =      X'01       ; WRITE VEHICLE PRESENCE DATUM
44 0000          ;
45 0000          ;
46 0000          ;
47 0000          ;
48 0000          ;
49 0000          ;
50 0000          ;
51 0000          ;
52 0000 0003 A FC03  =      X'03       ; FUNCTION CODE 03, STOP PULSE, RTC
53 0000 0005 A FC05  =      X'05       ; FUNCTION CODE 05, START PULSE, RTC
54 0000 0007 A FC07  =      X'07       ; FUNCTION CODE 07, RESET PULSE, RTC
55 0000          ;
56 0000          ;
57 0000          ;
58 0000          ;
59 0000 FFF4 A DM12  =     -12
60 0000 FFF9 A DM7   =     -7
61 0000 FFFC A DM4   =     -4
62 0000 FFFE A DM2   =     -2
63 0000 FFFF A DM1   =     -1
64 0000 0000 A D0    =      0
65 0000 0001 A D1    =      1
66 0000 0002 A D2    =      2
67 0000 0003 A D3    =      3
68 0000 0004 A D4    =      4
69 0000 0005 A D5    =      5
70 0000 0006 A D6    =      6
71 0000 0007 A D7    =      7
72 0000 0008 A D8    =      8
73 0000 0009 A D9    =      9
74 0000 000A A D10   =     10
75 0000 000B A D11   =     11
76 0000 000C A D12   =     12
77 0000 000D A D13   =     13
78 0000 000E A D14   =     14
79 0000 000F A D15   =     15
80 0000 0010 A D16   =     16
81 0000 0011 A D17   =     17
82 0000 0012 A D18   =     18
83 0000 0013 A D19   =     19

```

... A S S E M B L Y C O N S T A N T S ...

08-29-77

NOTE: FUNCTION CODES ENDING IN  
 6 CANNOT BE USED FOR RIN  
 INSTRUCTIONS DUE TO  
 CONFLICT WITH TTY ROUTINE

... D I S P L A C E M E N T C O N S T A N T S ...

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PBDU PRODUCTION PROTOTYPE  
ASSEMBLY CONSTANTS

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PAGE NUMBER 4

84	0000	0014	A	D20	=	20
85	0000	0015	A	D21	=	21
86	0000	0016	A	D22	=	22
87	0000	0017	A	D23	=	23
88	0000	0018	A	D24	=	24
89	0000	0019	A	D25	=	25
90	0000	001A	A	D26	=	26
91	0000	0074	A	D116	=	116
92	0000	0076	A	D118	=	118
93	0000					
94	0000	0010	A	DETS	=	16
95	0000					
96	0000					
97	0000					
98	0000					
99	0000					
100	0000					
101	0000	FF92	A	CM110	=	-110
102	0000	FF9C	A	CM100	=	-100
103	0000	FFEC	A	CM20	=	-20
104	0000	FFF0	A	CM16	=	-16
105	0000	FFF6	A	CM10	=	-10
106	0000	FFFA	A	CM6	=	-6
107	0000	FFFE	A	CM2	=	-2
108	0000	FFFF	A	CM1	=	-1
109	0000	0000	A	C0	=	0
110	0000	0001	A	C1	=	1
111	0000	0002	A	C2	=	2
112	0000	0003	A	C3	=	3
113	0000	0004	A	C4	=	4
114	0000	0005	A	C5	=	5
115	0000	0006	A	C6	=	6
116	0000	0007	A	C7	=	7
117	0000	0008	A	C8	=	8
118	0000	000F	A	C15	=	15
119	0000	0020	A	C32	=	32
120	0000	0030	A	C48	=	48
121	0000	007D	A	C125	=	125

; NUMBER OF DETECTORS  
; FOR PBDU PRODUCTION PROTOTYPE

... IMMEDIATE DATA CONSTANTS ...

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PBDU PRODUCTION PROTOTYPE  
ASSEMBLY CONSTANTS

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PAGE NUMBER 5

```

122 0000      .PAGE
123 0000      ;
124 0000      ;
125 0000      ;
126 0000 0001 A CCEZ      =      X'1      ; CONDITION CODE 1 (ACO).EG.0
127 0000 0002 A CCZP      =      X'2      ; CONDITION CODE 2 (ACO) ZERO, POSITIVE
128 0000 0003 A CCB0      =      X'3      ; CONDITION CODE 3 ACO BIT 0 = 1
129 0000 0004 A CCB1      =      X'4      ; CONDITION CODE 4 ACO BIT 1 = 1
130 0000 0005 A CCNZ      =      X'5      ; CONDITION CODE 5 (ACO).NE.0
131 0000 0008 A CCSF      =      X'8      ; CONDITION CODE 8 STACK FULL
132 0000 000B A CCZB      =      X'B      ; CONDITION CODE 11 (ACO).LE.0
133 0000 000C A CCCU      =      X'C      ; CONDITION CODE 12 CCU IN SYSTEM
134 0000 000D A CCPH      =      X'D      ; CONDITION CODE 13 INITIALIZATION
135 0000      ; PSUEDO HALT AND
136 0000      ; AUTORESTART CATCH
137 0000      ; ON THE FLY
138 0000 000E A CCCF      =      X'E      ; CONDITION CODE 14 CATCH ON THE FLY
139 0000 000F A CCAR      =      X'F      ; CONDITION CODE 15
140 0000      ; SELF TEST LAMPS
141 0000      ;
142 0000      ;
143 0000      ;
144 0000      ;
145 0000      ;
146 0000 0001 A INEN      =      1      ; NOTE : DANYL ( CCU ) USES FLAG-8
147 0000 0002 A SELF      =      2      ; INTERRUPT ENABLE FLAG
148 0000 0003 A MERR      =      3      ; SELECT FLAG
149 0000 0005 A ARST      =      5      ; MEMORY ERROR DETECTED
                                ; AUTO RESTART FLAG

```

REVISION-F 10/02/73  
PBDU PRODUCTION PROTOTYPE  
BASE PAGE

08/30/77 9.187  
PAGE NUMBER 6

```

152 0000      .LIST LBP
153 0000      ;
154 0000      ;
155 0000      ;
156 0000      ;
157 0000      ;
158 0000 2420 A      JMP      @AERSI
159 0001      ;
160 0001      ;
161 0001 2421 A      JMP      @AEGIS
162 0002      ;

```

... B A S E P A G E ...

2-7-77

... TRANSFER TO RESTART INITIALIZATION ROUTINE...

... TRANSFER TO GENERAL INTERRUPT SERVICING ROUTINE

REVISION-F 10/02/73  
PBDU PRODUCTION PROTOTYPE  
BASE PAGE - PROGRAM ENTRY POINTS

08/30/77 9.187  
PAGE NUMBER 7

```

165 0002      .LIST LBP
166 0002      ;
167 0002      .ASECT
168 0000 0020 A      .=X'20
169 0020 1000 A AERSI:    .WORD      ERSI      ; RESTART INITIALIZATION ROUTINE
170 0021 1023 A AEGIS:    .WORD      EGIS      ; GENERAL INTERRUPT SERVICING ROUTINE
171 0022 10A4 A AECCU:    .WORD      ECCU      ; CCU INITIALIZATION ROUTINE
172 0023 10C2 A AEMAD:    .WORD      EMAD      ; INITIAL RAM ADDRESS TEST ROUTINE
173 0024 1393 A AEBKD:    .WORD      EBKD      ; BACKGROUND PROGRAM MONITOR
174 0025 10A1 A AECER:    .WORD      ECER      ; CLOCK ERROR ROUTINE
175 0026 10CC A AESCH:    .WORD      ESCH      ; EXECUTIVE SCHEDULING ROUTINE
176 0027 10DD A AEADC:    .WORD      EADC      ; AUTORESTART ROUTINE
177 0028 10FE A AXRTC:    .WORD      XRTC      ; RTC DATA OUTPUT SEQUENCE ROUTINE
178 0029 1109 A ACOTF:    .WORD      COTF      ; CATCH ON THE FLY ROUTINE FOR CHECKOUT .....
179 002A      ;
180 002A      ;
181 002A      ;
182 002A 139F A ASMA:     .WORD      SMAD      ; RAM ADDRESS TEST

```

... SELF TEST ENTRY POINTS ...

```

185 002P          .LIST    LPP
186 002P 0068 A    .X'69
187 0068          ;
188 0068          ;
189 0068          ; DATA OUTPUT CPC DATA BASE POINTERS
190 0068          ;
191 0068 3080 A ABUSWD: .WORD    BUSWD          ; BUS PRESENT WORD LOCATION
192 0069 3081 A AVPREC: .WORD    VPREC          ;; VEHICLE PRESENT OUTPUT WORD LOCATION
193 006A 30B8 A APRSNT: .WORD    VPRSNT         ; VEHICLE PRESENT DATA WORD LOCATION
194 006B          ; USED BY VCLAS TO SAY IF VEHICLE PRESENT
195 006B 0079 A ADBIT:  .WORD    DBIT           ; TABLE OF BIT PATTERN SHOWING
196 006C          ; DETECTOR POSITION IN OUTPUT WORD
197 006C 3093 A ADCTR:  .WORD    DCTR           ; LOCATES COUNT SHOWING DETECTOR
198 006D          ; BEING EXAMINED
199 006D 3082 A ACTR:   .WORD    CTR            ; POINTER TO 16 COUNTERS, ONE PER DETECTOR
200 006E 0004 A BUSSET: .WORD    X'4           ; NO. CYCLES TO LEAVE BUS BIT SET
201 006F          ;
202 006F          ; ... VCLASS CPC- DATA BASE POINTERS ...
203 006F          ;
204 006F 1200 A AVCLAS: .WORD    VCLAS          ; VEHICLE CLASSIFICATION ROUTINE
205 0070 3000 A AVCSDB: .WORD    VCSDB         ; BUS SIGNATURE DATA BASE
206 0071 30A4 A AVCDB:  .WORD    VCSDB         ; VCLAS TEMP. STORAGE POINTER
207 0072          ; ( SIGNATURE DATA BASE COPIED HERE )
208 0072 3145 A APERR:  .WORD    PERR          ; VCLAS ERROR BUFFER POINTER
209 0073 30BA A AVCLOG: .WORD    VCLOG         ; BEGINNING LOC. OF VEHICLE LOG
210 0074 3094 A AVCVC:  .WORD    VCVC         ; VEHICLE COUNTERS ( 1 PER DETECTOR )
211 0075 0001 A EOSBIT: .WORD    X'1           ; END OF SIGNATURE BIT 1
212 0076 0100 A VPRES:  .WORD    X'100        ; VEHICLE PRESENT BIT 8
213 0077          ;
214 0077          ;EXECUTIVE CPC DATA BASE POINTERS
215 0077          ;
216 0077 30C6 A AEBUF:  .WORD    EBUF          ; BEGINNING LOC OF EXECUTIVE CPC DATA
217 0078          ; BASE
218 0078 1150 A ADMON:  .WORD    DMON         ; DETECTOR MONITOR, SCANS ALL SIGNATURES
219 0079 0010 A DBIT:   .WORD    DETS         ; NUMBER OF DETECTORS IN SYSTEM
220 007A          ; SHOWS BIT POSITIONS FOR EACH DETECTOR
221 007A          ; IN BOTH BUS AND VEHICLE PRESENT OUTPUT WORDS
222 007A 0001 A          .WORD    X'1          ; DETECTOR-1
223 007B 0002 A          .WORD    X'2          ; DETECTOR-2
224 007C 0004 A          .WORD    X'4          ; DETECTOR-3
225 007D 0008 A          .WORD    X'8          ; DETECTOR-4
226 007E 0010 A          .WORD    X'10         ; DETECTOR-5
227 007F 0020 A          .WORD    X'20         ; DETECTOR-6
228 0080 0040 A          .WORD    X'40         ; DETECTOR-7
229 0081 0080 A          .WORD    X'80         ; DETECTOR-8
230 0082 0100 A          .WORD    X'100        ; DETECTOR-9
231 0083 0200 A          .WORD    X'200        ; DETECTOR-10
232 0084 0400 A          .WORD    X'400        ; DETECTOR-11
233 0085 0800 A          .WORD    X'800        ; DETECTOR-12
234 0086 1000 A          .WORD    X'1000       ; DETECTOR-13
235 0087 2000 A          .WORD    X'2000       ; DETECTOR-14
36 0088 4000 A          .WORD    X'4000       ; DETECTOR-15

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BASE PAGE - DATA POINTERS

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237 0089 8000 A	•WORD	X*8000	; DETECTOR-16
238 008A			; END OF DBIT TABLE
239 008A 30B9 A ACLASS:	•WORD	CLASS	; TEMPORARY SAVE LOC. FOR VCLAS OUTPUT
240 008B			; BY DMON
241 008B 315A A AEERR:	•WORD	EERR	; ERROR BUFFER
242 008C			
243 008C 1188 A AERE0:	•WORD	ERE0	; ERROR RECORDING ROUTINE
244 008D 11C1 A AERE1:	•WORD	ERE1	; ERROR RECORDING ROUTINE
245 008E 11CA A AERE2:	•WORD	ERE2	; ERROR RECORDING ROUTINE
246 008F 11D3 A AERE3:	•WORD	ERE3	; ERROR RECORDING ROUTINE
247 0090 11DC A AERE4:	•WORD	ERE4	; ERROR RECORDING ROUTINE
248 0091 11E5 A AERE5:	•WORD	ERE5	; ERROR RECORDING ROUTINE
249 0092 11EE A AERE6:	•WORD	ERE6	; ERROR RECORDING ROUTINE
250 0093 11F7 A AERE7:	•WORD	ERE7	; ERROR RECORDING ROUTINE
251 0094			
252 0094			
253 0094			
254 0094			
255 0094 3187 A ADEND:	•WORD	DEND	; END LOCATION OF DATA BASE
256 0095 318C A ACTF:	•WORD	DEND+5	; FIRST LOCATION FOR CATCH ON THE FLY
257 0096			; ( DEBUG ) PROGRAM. LEAVES 5 UNTOUCHED
258 0096			; LOCATIONS AFTER DEND
259 0096 31EB A AERAM:	•WORD	DEND+100	; FIRST LOCATION IN FREE RAM FOR
260 0097			; MEMORY TESTING

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BASE PAGE - SAVE AREA POINTERS

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263 0097	•LIST	LRP	
264 0097			
265 0097 30C7 A AESAV:	•WORD	ESAV	; GENERAL INTERRUPT SAVE AREA POINTERS
266 0098 30C9 A AESV2:	•WORD	ESV2	
267 0099 30CB A AESVF:	•WORD	ESVF	
268 009A 30DC A AESVS:	•WORD	ESVS	
269 009B			
270 009B 30DD A ACSAV:	•WORD	CSAV	; SNAPSHOT SAVE AREA
271 009C 30DF A ACSV2:	•WORD	CSV2	
272 009D 30E1 A ACSVF:	•WORD	CSVF	
273 009E 30F2 A ACSVS:	•WORD	CSV5	
274 009F			
275 009F 30F5 A AISV2:	•WORD	ISV2	; STACK FULL SAVE AREA POINTERS
276 00A0 30F7 A AISTK1:	•WORD	ISTK1	
277 00A1 30F8 A AISTK2:	•WORD	ISTK2	
278 00A2 30F9 A AISTK3:	•WORD	ISTK3	
279 00A3 30FA A AISTK4:	•WORD	ISTK4	
280 00A4			
281 00A4 3109 A AEDSV2:	•WORD	EDSV2	; AUTORESTART SAVE AREA POINTERS
282 00A5 310B A AEDSVF:	•WORD	EDSVF	
283 00A6 311C A AEDSVS:	•WORD	EDSV5	
284 00A7			
285 00A7 311D A ACTST:	•WORD	CTST	; OPTIONAL USE SAVE AREA POINTER
286 00A8			
287 00A8			
288 00A8			... RAM ADDRESS TEST DATA POINTERS ...
289 00A8 3125 A ASSAD:	•WORD	SSAD	; RAM ADDRESS TEST START ADDRESS
290 00A9 3126 A ASEAD:	•WORD	SEAD	; RAM ADDRESS TEST END ADDRESS
291 00AA			

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BASE PAGE - PERIPHERAL DEVICE ADDRESSES

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294 00AA          .LIST   LRP
295 00AA 00E0 A    .='E0
296 00F0          ;
297 00F0          ; PERIPHERAL DEVICE ADDRESSES
298 00F0          ;
299 00E0 0400 A ARTC: .WORD   8 * 128      ; RTC DEVICE ADDRESS
300 00E1 0500 A ACUM: .WORD  10 * 128      ; OUTPUT REGISTERS FOR
301 00E2          ; VEHICLE PRESENCE, BUS DETECTED
302 00E2 1F80 A ACCU: .WORD  63*128        ; CCU DEVICE ADDRESS
303 00E3          ;
304 00E3          ;

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BASE PAGE - COMMON HEXADECIMAL CONSTANTS

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307 00E3          .LIST   LBP
308 00E3 00F0 A    .='F0
309 00F0          ;
310 00F0          ;
311 00F0 3300 A H3300: .WORD   X'3300      ... COMMON HEXADECIMAL CONSTANTS ...
312 00F1 33CF A H33CF: .WORD   X'33CF      ; START ADDRESS OF UNUSED CCU RAM
313 00F2 0200 A H0200: .WORD   X'0200      ; END ADDRESS OF UNUSED CCU RAM
314 00F3 32FF A H32FF: .WORD   X'32FF      ; RTS DO INSTRUCTION
                                     ; END ADDRESS FOR RTC RAM ADDRESS TEST

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EXECUTIVE CPC - RESTART INITIALIZATION

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319 1000      .LIST   LER
320 1000      ;
321 1000      ;
322 1000      ;
323 1000      ;
324 1000      ;
325 1000      ;
326 1000 1842 A ERSI:  ROC   CCSF,ESTK      ; TEST FOR STACKFULL LINE = 1
327 1001      ;                               STACK SHOULD NOT BE FULL
328 1001 8CE0 A      LD    AC3,ARTC
329 1002 4C00 A      LI    AC0,C0
330 1003 0603 A      ROUT   FC03      ; ASSURE RTC STOPPED
331 1004 0607 A      ROUT   FC07      ; ASSURE RTC INTERRUPT PULSE RESET
332 1005      ;
333 1005 0980 A      PFLG   INFN      ; DISABLE INTERRUPTS
334 1006      ;
335 1006      ;
336 1006 2C22 A      JSR    @AECCU      ... INITIALIZE CCU SERVICING ROUTINE ...
337 1007      ;
338 1007      ;
339 1007 0714 A      CLRST  D4      ... INITIALIZE RAM ERROR STATUS FLAG ...
340 1008 2C23 A      JSR    @AEMAD      ; CLEAR MEMORY ADDRESS TEST STATUS FLAG
341 1009      ;                               D5,D6,D7 ARE SPARES
342 1009 0715 A      CLRST  D5
343 100A 0716 A      CLRST  D6
344 100B 0717 A      CLRST  D7
345 100C      ;
346 100C      ;
347 100C 80F2 A      LD    AC0,H0200      ... INITIALIZE COTF ...
348 100D B095 A      ST     AC0,@ACTF      ; RTS DO INSTRUCTION
349 100E      ;                               ; STORE IN FIRST LOCATION OF DEBUG RAM AREA
350 100E      ;                               ; (ENTRY POINT VIA COTF)
351 100E      ;
352 100E      ;
353 100E 4EF0 A      LI     AC2,CM16      ... INITIALIZE CPU STACK ...
354 100F 4700 A      PULL   AC3      ; PULL 16 WORDS FROM STACK
355 1010 4A01 A      AISZ   AC2,C1
356 1011 21FD A      JMP    *-2
357 1012      ;
358 1012      ;
359 1012 4FFF A      LI     AC3,CM1      ... INITIALIZE STACK FOR BACKGROUND ROUTINES ...
360 1013 4300 A      PUSH   AC3
361 1014 4300 A      PUSH   AC3      ; PUSH TWO PROTECTION WORDS OF ALL ONES
362 1015      ;                               TO INSURE INTERRUPT ON STACK FULL
363 1015      ;
364 1015      ;
365 1015      ;
366 1015 4C00 A      LI     AC0,C0      ZERO DATA BASE FROM VCSDB TO DEND
367 1016 8870 A      LD     AC2,AVCSDB
368 1017 A200 A      ST     AC0,(AC2)
369 1018 4A01 A      AISZ   AC2,C1
370 1019 2100 A      JMP    *-1
EZDB:

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371 101A E894 A      SKG      AC2,ADEND
372 101B 21FB A      JMP      EZDB
373 101C              ;
374 101C              ;
375 101C              ;
376 101C 1DFF A EHLT:  BOC      ... INITIALIZATION PSEUDO HALT ...
                               CCPH,EHLT      ; PSEUDO HALT LOOP
377 101D              ;
378 101D              ;
379 101D 4C01 A      LI        AC0,C1
380 101E 8CE0 A      LD        AC3,ARTC
381 101F 0605 A      ROUT      FC05      ; START RTC
382 1020              ;
383 1020              ;
384 1020 8C24 A      LD        AC3,AEBKD      ... INITIATE BACKGROUND PROGRAMS ...
385 1021 4300 A      PUSH      AC3
386 1022              ; STACK ADDRESS NOW IS FOR THE BACKGROUND
387 1022              ; PROGRAMS
388 1022              ;
389 1022 0100 A      RTI        DO      ; RETURN & ENABLE *RUPTS
390 1023              ; (IE; GO TO BACKGROUND PROGRAMS )
```

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393 1023          •LIST  LER
394 1023          ;
395 1023          ;
396 1023          EGIS:      ... GENERAL INTERRUPT SERVICING ROUTINE ...
397 1023 181F A      BOC      CCSF,ESTK      ; TEST FOR STACK FULL LINE = 1
398 1024          ;
399 1024 8898 A      ST        AC2,@AESV2      ; SAVE ACCUMULATORS
400 1025 8898 A      LD        AC2,AESV2
401 1026 A2FE A      ST        AC0,DM2(AC2)
402 1027 A6FF A      ST        AC1,DM1(AC2)
403 1028 AE01 A      ST        AC3,D1(AC2)
404 1029          ;
405 1029 4400 A      PULL      AC0              ; SAVE RALU FLAGS
406 102A 0080 A      PUSHF
407 102B 5400 A      XCHRS      AC0
408 102C B099 A      ST        AC0,@AESVF
409 102D          ;
410 102D 4D04 A      LI        AC1,C4          ; SAVE CPU STACK
411 102E 8899 A      LD        AC2,AESVF      ; STACK FOLLOWS RALU FLAG WORD
412 102F 4700 A      EGIS1:   PULL      AC3      ; PULL STACK FROM TOP TO BOTTOM
413 1030 AE01 A      ST        AC3,D1(AC2)
414 1031 4700 A      PULL      AC3
415 1032 AE02 A      ST        AC3,D2(AC2)
416 1033 4700 A      PULL      AC3
417 1034 AE03 A      ST        AC3,D3(AC2)
418 1035 4700 A      PULL      AC3
419 1036 AE04 A      ST        AC3,D4(AC2)
420 1037 4A04 A      AISZ      AC2,D4          ; INCREMENT SAVE AREA ADDRESS BY 4
421 1038 49FF A      AISZ      AC1,CM1        ; DECREMENT PASS COUNTER, SKIP IF DONE
422 1039 21F5 A      JMP      EGIS1
423 103A          ;
424 103A          ;
425 103A 4C01 A      LI        AC0,C1          ; SAVE SELECT FLAG STATE
426 103B 58EF A      ROR      AC0,D17
427 103C 1303 A      BOC      CCB0,EGIS2      ; BRANCH IF SELECT FLAG SET
428 103D 4C00 A      LI        AC0,C0
429 103E B09A A      ST        AC0,@AESVS      ; SELECT FLAG = 0
430 103F 212D A      JMP      ERTC
431 1040 4C01 A      EGIS2:   LI        AC0,C1
432 1041 B09A A      ST        AC0,@AESVS      ; SELECT FLAG = 1
433 1042 212A A      JMP      ERTC
434 1043          ;
435 1043          ;
436 1043          ;
437 1043          ;
438 1043          ESTK:      ... CLEAR STACK FULL CONDITION ...
439 1043 5400 A      XCHRS      AC0
440 1044 B0A0 A      ST        AC0,@AISTK1      ; SAVE STACK 1
441 1045 4400 A      PULL      AC0              ; RESTORE AC0
442 1046 5400 A      XCHRS      AC0
443 1047 B0A1 A      ST        AC0,@AISTK2      ; SAVE STACK 2
444 1048 4400 A      PULL      AC0              ; RESTORE AC0

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445	1049	5400	A	XCHRS	ACO	
446	104A	B0A2	A	ST	ACO,@AISTK3	; SAVE STACK 3
447	104B	4400	A	PULL	ACO	; RESTORE ACO
448	104C	5400	A	XCHRS	ACO	
449	104D	B0A3	A	ST	ACO,@AISTK4	; SAVE STACK 4
450	104E	4400	A	PULL	ACO	; RESTORE ACO
451	104F					
452	104F	B89F	A	ST	AC2,@AISV2	; SAVE ACCUMULATORS
453	1050	889F	A	LD	AC2,AISV2	
454	1051	A2FE	A	ST	ACO,DM2(AC2)	
455	1052	A6FF	A	ST	AC1,DM1(AC2)	
456	1053	AE01	A	ST	AC3,D1(AC2)	
457	1054					
458	1054	8CE0	A	LD	AC3,ARTC	
459	1055	4C00	A	LI	ACO,C0	
460	1056	0603	A	ROUT	FC03	; STOP RTC
461	1057	0980	A	PFLG	INEN	; DISABLE INTERRUPTS
462	1058					
463	1058	88A3	A	LD	AC2,AISTK4	; SAVE STACK 5 - 16
464	1059	4D03	A	LI	AC1,C3	
465	105A	4700	A	PULL	AC3	
466	105B	AE01	A	ST	AC3,D1(AC2)	
467	105C	4700	A	PULL	AC3	
468	105D	AE02	A	ST	AC3,D2(AC2)	
469	105E	4700	A	PULL	AC3	
470	105F	AE03	A	ST	AC3,D3(AC2)	
471	1060	4700	A	PULL	AC3	
472	1061	AE04	A	ST	AC3,D4(AC2)	
473	1062	4A04	A	AISZ	AC2,C4	
474	1063	49FF	A	AISZ	AC1,CM1	
475	1064	21F5	A	JMP	ESTK1	
476	1065					
477	1065	889F	A	LD	AC2,AISV2	; RESTORE ACCUMULATORS
478	1066	82FE	A	LD	ACO,DM2(AC2)	
479	1067	86FF	A	LD	AC1,DM1(AC2)	
480	1068	8E01	A	LD	AC3,D1(AC2)	
481	1069	989F	A	LD	AC2,@AISV2	
482	106A					
483	106A	2C27	A	JSR	@AEADC	; AUTORESTART ROUTINE, NO RETURN
484	106B					
485	106B	2100	A	JMP	.+1	; THIS INST SHOULD NEVER BE REACHED
486	106C	21FE	A	JMP	.-1	



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487 106D          ; PAGE
488 106D          ;
489 106D          ;
490 106D          ;
491 106D          ;
492 106D          ;
493 106D          ;
494 106D          ;
495 106D          ;
496 106D 8877 A   ERTC: LD   AC2,AERUF      ; CHECK FOR COMPLETION OF PREVIOUS
497 106E 8200 A   LD   AC0,D0(AC2)      ;   RTC COMPUTE SEQUENCE
498 106F 110A A   BOC   CCEZ,ERTC1      ; BRANCH IF NO ERROR
499 1070          ;
500 1070 888B A   LD   AC2,AEERR        ;
501 1071 A202 A   ST   AC0,D2(AC2)      ; STORE RTC COMPUTE FLAG, EERRO
502 1072 8201 A   LD   AC0,D1(AC2)
503 1073 4801 A   AISZ  AC0,C1          ; INCREMENT ERROR COUNTER
504 1074 2100 A   JMP   .+1
505 1075 A201 A   ST   AC0,D1(AC2)
506 1076 8200 A   LD   AC0,D0(AC2)
507 1077 0720 A   SETBIT D0            ; SET ERROR FLAG BIT 0
508 1078 A200 A   ST   AC0,D0(AC2)
509 1079 2425 A   JMP   @AECER          ; RTC ERROR RESPONSE ROUTINE
510 107A          ;
511 107A 4C01 A   ERTC1: LI   AC0,C1      ; SET RTC COMPUTE FLAG
512 107B A200 A   ST   AC0,D0(AC2)
513 107C          ;
514 107C          ;
515 107C 4FFF A   LI   AC3,CM1
516 107D 4300 A   PUSH  AC3
517 107E 4300 A   PUSH  AC3            ; PUSH TWO PROTECTION WORDS OF ALL ONES
518 107F          ;
519 107F 2C26 A   JSR   @AESCH          ; CALL SCHEDULING ROUTINE
520 1080          ;
521 1080 4700 A   PULL  AC3            ; PULL TWO PROTECTION WORDS FROM STACK
522 1081 4700 A   PULL  AC3
523 1082          ;
524 1082          ;
525 1082          ;
526 1082          ;
527 1082 8877 A   LD   AC2,AEBUF        ; RESET RTC COMPUTE FLAG
528 1083 4C00 A   LI   AC0,C0
529 1084 A200 A   ST   AC0,D0(AC2)
530 1085          ;
531 1085          ;
532 1085 909A A   LD   AC0,@AESVS       ; RESTORE COMPUTATIONAL ENVIRONMENT ...
533 1086 1102 A   BOC   CCEZ,EGIS4     ; RESTORE SELECT FLAG
534 1087 0A00 A   SFLG  SELF
535 1088 2101 A   JMP   .+2
536 1089 0A80 A   EGIS4: PFLG  SELF
537 108A          ;
538 108A          ;

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539 108A 4D04 A      LI      AC1,C4      ; RESTORE CPU STACK
540 108B 889A A      LD      AC2,AESVS   ; STACK PRECEDES SELECT FLAG WORD
541 108C 4AFC A EGIS5: AISZ   AC2,DM4    ; DECREMENT SAVE AREA ADDRESS BY 4
542 108D 8E03 A      LD      AC3,D3(AC2) ; PUSH STACK FROM BOTTOM TO TOP
543 108E 4300 A      PUSH    AC3
544 108F 8E02 A      LD      AC3,D2(AC2)
545 1090 4300 A      PUSH    AC3
546 1091 8E01 A      LD      AC3,D1(AC2)
547 1092 4300 A      PUSH    AC3
548 1093 8E00 A      LD      AC3,D0(AC2)
549 1094 4300 A      PUSH    AC3
550 1095 49FF A      AISZ   AC1,CM1     ; DECREMENT PASS COUNTER, SKIP IF DONE
551 1096 21F5 A      JMP     EGIS5
552 1097          ;
553 1097 9099 A      LD      ACO,@AESVF   ; RESTORE PALU FLAGS
554 1098 5400 A      XCHRS  ACO
555 1099 0280 A      PULLF
556 109A 4000 A      PUSH    ACO
557 109B          ;
558 109B          ; RESTORE ACCUMULATORS
559 109B 8898 A      LD      AC2,AESV2
560 109C 82FE A      LD      ACO,DM2(AC2)
561 109D 86FF A      LD      AC1,DM1(AC2)
562 109E 8E01 A      LD      AC3,D1(AC2)
563 109F 9898 A      LD      AC2,@AESV2
564 10A0          ;
565 10A0 0100 A      RTI      ; RETURN AND ENABLE INTERRUPTS
566 10A1          ;
567 10A1          ; ... RTC ERROR, PREVIOUS SEQUENCE INCOMPLETE ...
568 10A1          ECER:
569 10A1 2C27 A      JSR     @AEADC      ; AUTORESTART ROUTINE, NO RETURN
570 10A2          ;
571 10A2 2100 A      JMP     .+1        ; THIS INST SHOULD NEVER BE REACHED
572 10A3 21FE A      JMP     .-1

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575 10A4          .LIST   LFR
576 10A4          ;
577 10A4          ;
578 10A4          ECCU:
579 10A4          ;
580 10A4          ;
581 10A4 1C01 A    BOC     CCCU,+.2      ; BRANCH IF CCU IS IN SYSTEM
582 10A5 2115 A    JMP     ECCUR         ; JUMP IF CCU NOT IN SYSTEM
583 10A6          ;
584 10A6 9115 A    LD      ACO,@ACCU1    ; CHECK FIRST INST IN CCU ROUTINE
585 10A7 F115 A    SKNE    ACO,ECCU1    ; SKIP IF CCU NOT IN SYSTEM
586 10A8 2101 A    JMP     .+2
587 10A9 2111 A    JMP     ECCUR         ; JUMP TO RETURN
588 10AA          ;
589 10AA          ;
590 10AA 4C00 A    LI      ACO,C0
591 10AB 4D30 A    LI      AC1,C49      ; LENGTH OF CCU RAM = 48
592 10AC 8913 A    LD      AC2,ACWAP    ; INITIALIZE ADDRESS POINTER
593 10AD          ;
594 10AD A2F4 A    ECCU1: ST      ACO,DM12(AC2) ; CLEAR RAM
595 10AE 4A01 A    AISZ    AC2,C1      ; INCREMENT ADDRESS POINTER
596 10AF 49FF A    AISZ    AC1,CM1     ; DECREMENT COUNTER, SKIP IF DONE
597 10B0 21FC A    JMP     ECCU1      ; CONTINUE LOOP
598 10B1          ;
599 10B1 890E A    LO      AC2,ACWAP    ; INITIALIZE ADDRESS POINTER
600 10B2 7AF9 A    ISZ     DM7(AC2)    ; SET STATE WORD = +1
601 10B3 7E0C A    DSZ     O12(AC2)    ; SET BREAKPOINT ADDRESS 0 = -1
602 10B4 7E0E A    OSZ     D14(AC2)    ; SET BREAKPOINT ADDRESS 1 = -1
603 10B5          ;
604 10B5 810B A    LD      ACO,AECCUR   ; RETURN ADDRESS FROM CCU ROUTINE
605 10B6 A203 A    ST      ACO,D3(AC2)  ; STORE IN TEMPORARY PC LOC IN CCU RAM
606 10B7          ;
607 10B7 8107 A    LD      ACO,ACRAM    ; BASE ADDRESS OF CCU RAM WORK AREA
608 10B8 A2FA A    ST      ACO,CM6(AC2) ; INITIALIZE PUSH/PULL POINTER
609 10B9          ;
610 10B9 4C00 A    LI      ACO,C0      ; ACO = 0, INITIAL DISPLAY
611 10BA 2503 A    JMP     @ACDISP      ; TO CCU ROUTINE, RETURN IS TO ECCUR
612 10BB          ;
613 10BB 0200 A    ECCUP: RTS     D0      ; RETURN FROM ECCU
614 10BC          ;
615 10BC          ;
616 10BC EF00 A    ACCU1: .WORD   X'EF00 ; LOC OF FIRST INST IN CCU ROUTINE
617 10BD 86F7 A    ECCU1: .WORD   X'86F7 ; FIRST INST IN CCU ROUTINE
618 10BE EF85 A    ACDISP: .WORD   X'EF85 ; CCU ROM+X'85
619 10BF 3300 A    ACRAM: .WORD   X'33D0 ; FIRST LOCATION IN CCU RAM WORK AREA
620 10C0 330C A    ACWAP: .WORD   X'33DC ; CCU RAM WORK AREA+X'C
621 10C1 10B8 A    AECCUR: .WORD   ECCUR ; RETURN ADDRESS FROM CCU INITIALIZATION

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624 10C2      .LIST  LER
625 10C2      ;
626 10C2      ;          ... INITIALIZATION RAM ADDRESS TEST ...
627 10C2      EMAD:
628 10C2      ;
629 10C2      ;
630 10C2      ;          ... TEST 4K STATIC RAM ...
631 10C2 8096 A      LD      AC0,AERAM      (CAN ONLY TEST ADDRESS -NOT- USED BY DATA BASE)
632 10C3 B0A8 A      ST      AC0,@ASSAD      ; START ADDRESS ( PAST DATA BASE )
633 10C4 80F3 A      LD      AC0,H32FF      ; END ADDRESS ( JUST BEFORE CCU RAM )
634 10C5 B0A9 A      ST      AC0,@ASEAD
635 10C6      ;
636 10C6 2C2A A      JSR      @ASMAD
637 10C7 2101 A      JMP      EMAD          ; ERROR RETURN, (AC2) = CONTENTS
638 10C8      ;                          ; (AC3) = ADDRESS
639 10C8 0200 A      RTS      D0          ; RETURN FROM EMAD
640 10C9      ;                          ; NO ERROR
641 10C9 2C27 A EMAD: JSR      @AEADC      ; AUTORESTART ROUTINE, NO RETURN
642 10CA      ;
643 10CA 2100 A      JMP      .+1          ; THIS INST SHOULD NEVER BE REACHED
644 10CB 21FE A      JMP      .-1
645 10CC      ;
646 10CC      ;

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REVISION-F 10/02/73  
PBDU PRODUCTION PROTOTYPE  
EXECUTIVE CPC - SCHEDULING ROUTINE FOR RTC SEQUENCE

08/30/77 9.187  
PAGE NUMBER 21

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649 10CC      .LIST  LER
650 10CC      ;
651 10CC      ;          ... RTC SCHEDULING ROUTINE ...
652 10CC      ESCH:
653 10CC 8CE0 A      LD      AC3,ARTC
654 10CD 4C00 A      LI      AC0,C0          ; CLEAR AC0
655 10CE 0607 A      ROUT     FC07          ; RESET RTC INTERRUPT PULSE
656 10CF      ;
657 10CF 0900 A      SFLG     INEN          ; ENABLE INTERRUPTS
658 10D0      ;
659 10D0 1E01 A      BOC      CCCF,.,+2      ; BRANCH IF COTF JUMP CONDITION SET
660 10D1 2101 A      JMP      .+2
661 10D2 2C29 A      JSR      @ACOTF      ; CALL CATCH ON THE FLY ROUTINE
662 10D3      ;
663 10D3 2C78 A      JSR      @ADMON      ; CALL DETECTOR MONITOR TO
664 10D4      ;                          ; SCAN ALL SIGNATURES
665 10D4 2C28 A      JSR      @AXRTC      ; OUTPUT VEHICLE, BUS PRESENCE
666 10D5      ;
667 10D5 2105 A      JMP      ERTS
668 10D6      ;
669 10D6 8905 A      LD      AC2,EDLAY
670 10D7 5C76 A      SHL      AC0,D118
671 10D8 5C74 A      SHL      AC0,D116
672 10D9 4A01 A      AISZ     AC2,C1
673 10DA 21FC A      JMP      .-3
674 10DB      ;
675 10DB 0200 A ERTS: RTS      D0
676 10DC      ;          VARIABLE DELAY
677 10DC FFCE A EDLAY: .WORD  -50
678 10DD      ;
679 10DD      ;

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682 10CD          .LIST  LER
683 10CD          ;
684 10CD          ;      ... AUTORESTART ROUTINE ...
685 10DD          ;
686 10DD          EADC:
687 10CD          ;
688 10DD 88A4 A    ST      AC2,@AEDSV2      ; SAVE ACCUMULATORS
689 10DE 88A4 A    LD      AC2,AEDSV2
690 10DF A2FE A    ST      AC0,DM2(AC2)
691 10E0 A6FF A    ST      AC1,DM1(AC2)
692 10E1 AE01 A    ST      AC3,D1(AC2)
693 10E2          ;
694 10E2 8CE0 A    LD      AC3,ARTC
695 10E3 4C00 A    LI      AC0,C0
696 10F4 0603 A    ROUT    FC03            ; STOP RTC
697 10E5 0607 A    ROUT    FC07            ; ASSURE RTC INTERRUPT PULSE' RESET
698 10E6 0980 A    PFLG    INEN            ; DISABLE INTERRUPTS
699 10E7          ;
700 10E7 4400 A    PULL    AC0            ; SAVE RALU FLAGS
701 10E8 0080 A    PUSHF
702 10E9 5400 A    XCHRS  AC0
703 10EA 80A5 A    ST      AC0,@AEDSVF
704 10EB          ;
705 10EB 4D04 A    LI      AC1,C4          ; SAVE CPU STACK
706 10EC 88A5 A    LD      AC2,AEDSVF      ; STACK FOLLOWS RALU FLAG WORD
707 10ED 4700 A    EADC1: PULL    AC3      ; PULL STACK FROM TOP TO BOTTOM
708 10EE AE01 A    ST      AC3,D1(AC2)
709 10EF 4700 A    PULL    AC3
710 10F0 AE02 A    ST      AC3,D2(AC2)
711 10F1 4700 A    PULL    AC3
712 10F2 AE03 A    ST      AC3,D3(AC2)
713 10F3 4700 A    PULL    AC3
714 10F4 AE04 A    ST      AC3,D4(AC2)
715 10F5 4A04 A    AISZ    AC2,D4          ; INCREMENT SAVE AREA ADDRESS BY 4
716 10F6 49FF A    AISZ    AC1,CM1        ; DECREMENT PASS COUNTER, SKIP IF DONE
717 10F7 21F5 A    JMP     EADC1
718 10F8 1D01 A    BOC     CCPH,.,+2      ; BRANCH IF COTF SET; IE,
719 10F9          ; PSUEDO HALT SET
720 10F9 2101 A    JMP     .+2            ; NOT SET
721 10FA 2C29 A    JSR     @ACOTF         ; CALL CATCH ON THE FLY
722 10FB          ;
723 10FB          ;      ... LIGHT INDICATOR...
724 10FB 0D80 A    PFLG    ARST          ; SHOWS ROUTINE ENTERED
725 10FC          ; EXTERNAL HARDWARE MUST
726 10FC          ; FORCE SYSTEM INITIALIZATION
727 10FC          ; FLAG 13, FAULT-2 LITE
728 10FC 3081 A    NOP
729 10FD 21FE A    JMP     .-1            ; WAIT SYSTEM INITIALIZE VIA EXTERNAL SIGNAL

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REVISION-F 10/02/73  
PBDU PRODUCTION PROTOTYPE  
EXECUTIVE CPC-DATA OUTPUT

08/30/77 9.187  
PAGE NUMBER 23

```
732 10FE          .LIST LFX
733 10FE          ;
734 10FE          ;
735 10FE          ; ... OUTPUT DATA ...
736 10FE          XRTC:
737 10FE 8CE1 A    LD      AC3,ACMU      ; OUTPUT REGISTER DEVICE ADDRESS
738 10FF 1F05 A    BOC      CCAR,VTEST   ; BRANCH IF SET TO DO LAMP TEST
739 1100 9068 A    LD      AC0,@ABUSWD   ; BUS PRESENT WORD
740 1101 0600 A    ROUT     FC0
741 1102 9069 A    LD      AC0,@AVPREC    ; VEHICLE PRESENT WORD
742 1103 0601 A    ROUT     FC1
743 1104 0200 A    RTS      D0            ; RETURN FROM XRTC
744 1105          ;
745 1105          ; ... SELF TEST LAMPS ...
746 1105          ;
747 1105 4CFF A    VTEST: LI      AC0,CM1  ; ALL ONES OUTPUT
748 1106 0601 A    ROUT     FC1            ; LAMPS RETURN TO ORIGINAL STATE
749 1107 0600 A    ROUT     FC0            ; AFTER VTEST SWITCH IS RESET
750 1108 0200 A    RTS      D0
751 1109          ;
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754 1109          .LIST   LER
755 1109          ;
756 1109          ;
757 1109          ;... TIME OUT FOR DEBUG ROUTINE ...
758 1109          ;*****
759 1109          ;
760 1109          ;... CATCH ON THE FLY ...
761 1109          ;
762 1109          ;
763 1109          COTF:
764 1109 889C A      ST      AC2,@ACSV2          ; SAVE ACCUMULATORS
765 110A 889C A      LD      AC2,ACSV2
766 110B A2FE A      ST      AC0,DM2(AC2)
767 110C A6FF A      ST      AC1,DM1(AC2)
768 110D AE01 A      ST      AC3,D1(AC2)
769 110E          ;
770 110E 4400 A      PULL     AC0          ; SAVE RALU FLAGS
771 110F 0080 A      PUSHF
772 1110 5400 A      XCHRS   AC0
773 1111 B09D A      ST      AC0,@ACSVF
774 1112          ;
775 1112 4D04 A      LI      AC1,C4          ; SAVE CPU STACK
776 1113 889D A      LD      AC2,ACSVF      ; STACK FOLLOWS RALU FLAG WORD
777 1114 4700 A      COTF1: PULL     AC3      ; PULL STACK FROM TOP TO BOTTOM
778 1115 AE01 A      ST      AC3,D1(AC2)
779 1116 4700 A      PULL     AC3
780 1117 AE02 A      ST      AC3,D2(AC2)
781 1118 4700 A      PULL     AC3
782 1119 AE03 A      ST      AC3,D3(AC2)
783 111A 4700 A      PULL     AC3
784 111B AE04 A      ST      AC3,D4(AC2)
785 111C 4A04 A      AISZ     AC2,D4          ; INCREMENT SAVE AREA ADDRESS BY 4
786 111D 49FF A      AISZ     AC1,CM1        ; DECREMENT PASS COUNTER, SKIP IF DONE
787 111E 21F5 A      JMP      COTF1
788 111F          ;
789 111F          ;
790 111F 4C01 A      LI      AC0,C1          ; SAVE SELECT FLAG STATE
791 1120 58EF A      ROR      AC0,D17
792 1121 1303 A      BOC      CCR0,COTF2      ; BRANCH IF SELECT FLAG SET
793 1122 4C00 A      LI      AC0,C0
794 1123 B09E A      ST      AC0,@ACSVS      ; SELECT FLAG = 0
795 1124 2102 A      JMP      COTF3
796 1125 4C01 A      COTF2: LI      AC0,C1
797 1126 B09E A      ST      AC0,@ACSVS      ; SELECT FLAG = 1
798 1127          ;
799 1127          ;
800 1127          ; STOP THE CLOCK
801 1127 8CE0 A      COTF3: LD      AC3,ARTC
802 1128 4C00 A      LI      AC0,C0
803 1129 0603 A      ROUT     FC03          ; STOP RTC
804 112A 0607 A      ROUT     FC07          ; ASSURE RTC INTERRUPT PULSE RESET
805 112B          ;

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806 112B ;-----
807 112B 3081 A      NOP      ; INSEPT DEBUG HALT OR SNAP HERE
808 112C 3081 A      NOP
809 112D 2C95 A      JSR      @ACTF      ; FIRST LOCATION IN DEBUG AREA RAM
810 112E      ;      ; (AFTER DFND, BUT BEFORE RAM TEST AREA )
811 112E 3081 A      NOP
812 112F 3081 A      NOP
813 1130 3081 A      NOP
814 1131 ;-----
815 1131 ;
816 1131 ;
817 1131 8CE0 A      LD      AC3,ARTC      START THE CLOCK
818 1132 4C00 A      LI      AC0,C0
819 1133 0605 A      ROUT     FC05      ; START RTC
820 1134 ;
821 1134 ;      ... RESTORE COMPUTATIONAL ENVIRONMENT ...
822 1134 ;
823 1134 909E A      LD      AC0,@ACSVS      ; RESTORE SELECT FLAG
824 1135 1102 A      BOC     CCEZ,COTF4
825 1136 0A00 A      SFLG     SELF      ; SET SELECT FLAG
826 1137 2101 A      JMP     .+2
827 1138 0A80 A      COTF4: PFLG     SELF      ; RESET SELECT FLAG
828 1139 ;
829 1139 ;
830 1139 4D04 A      LI      AC1,C4      ; RESTORE CPU STACK
831 113A 889E A      LD      AC2,ACSVS      ; STACK PRECEDES SELECT FLAG WORD
832 113B 4AFC A      COTF5: AISZ     AC2,DM4      ; DECREMENT SAVE AREA ADDRESS BY 4
833 113C 8E03 A      LD      AC3,D3(AC2)      ; PUSH STACK FROM BOTTOM TO TOP
834 113D 4300 A      PUSH     AC3
835 113E 8E02 A      LD      AC3,D2(AC2)
836 113F 4300 A      PUSH     AC3
837 1140 8E01 A      LD      AC3,D1(AC2)
838 1141 4300 A      PUSH     AC3
839 1142 8E00 A      LD      AC3,D0(AC2)
840 1143 4300 A      PUSH     AC3
841 1144 49FF A      AISZ     AC1,CM1      ; DECREMENT PASS COUNTER, SKIP IF DONE
842 1145 21F5 A      JMP     COTF5
843 1146 ;
844 1146 909D A      LD      AC0,@ACSVF      ; RESTORE RALU FLAGS
845 1147 5400 A      XCHRS     AC0
846 1148 0280 A      PULLF
847 1149 4000 A      PUSH     AC0
848 114A ;
849 114A ;      RESTORE ACCUMULATORS
850 114A 889C A      LD      AC2,ACSV2
851 114B 82FE A      LD      AC0,DM2(AC2)
852 114C 86FF A      LD      AC1,DM1(AC2)
853 114D 8E01 A      LD      AC3,D1(AC2)
854 114E 989C A      LD      AC2,@ACSV2
855 114F ;
856 114F 0200 A      RTS      D0      ; RETURN FROM COTF

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859 1150          .LIST LDM
860 1150          ; ... LOOP DETECTOR SIGNATURE SEQUENCER ...
861 1150          ; SEQUENCES THRU SIGNATURES 1 TO 16
862 1150          ; CALLS VCLAS TO EXAMINE SIGNATURE DATA
863 1150          ; VEHICLE PRESENT BIT WILL BE SET/RESET AND STORED IN
864 1150          ; THE OUTPUT WORD ' VPREC '. BUS DETECTED BIT WILL
865 1150          ; BE STORED IN THE OUTPUT WORD ' BUSWORD '.
866 1150          ; A DELAY IS PROVIDED FOR IN RESETTING
867 1150          ; EACH BIT IN ' BUSWORD '.
868 1150          ;
869 1150          ;
870 1150 4C00 A DMON: LI ACO,DO ; INITIALIZE COUNTER TO ALLOW
871 1151          ; LOOPING FOR CHECKING DETECTOR SIGNATURES
872 1151          ; ( PRESENTLY 16 DETECTORS )
873 1151 B06C A DMORE: ST ACO,@ADCTR ; SAVE CURRENT DETECTOR INDEX
874 1152          ; ENTRY POINT FOR LOOPING 15 MORE TIMES
875 1152          ; CURRENT DETECTOR INDEX
876 1152 906C A LD ACO,@ADCTR ;
877 1153 4801 A AISZ ACO,C1 ;ACO=ACO+1
878 1154 B06C A ST ACO,@ADCTR ; SAVE CURRENT DETECTOR INDEX
879 1155 E079 A SKG ACO,DBIT ; SEE IF (ACO) > NO. DETECTORS)
880 1156          ; TO BE CHECKED( PRESENTLY 16 )
881 1156 2101 A JMP DMORE1 ; HERE IF NOT >
882 1157 0200 A RTS DO ; HERE IF >, RETURN FROM DMON
883 1158          ;
884 1158 DMORE1:
885 1158 2C6F A JSR @AVCLAS ; ENTER WITH ACO=DETECTOR TO EXAMINE
886 1159          ; VEHICLE CLASSIFIER RETURNS VIA DO OR D1
887 1159 210C A JMP CLASFID ; HERE FOR SIGNATURE CLASSIFIED BY VCLAS
888 115A          ;
889 115A          ; HERE FOR VEHICLE WAS NOT CLASSIFIED BY VCLAS
890 115A          ; SET OR RESET VEHICLE PRESENT BIT IN OUTPUT WORD
891 115A 986C A LD AC2,@ADCTR ; FIND CURRENT DETECTOR
892 115B 8279 A LD ACO,DBIT(AC2) ; INDEX THRU DBIT TABLE
893 115C 3381 A RCPY ACO,AC3 ; COPY ACO TO AC3
894 115D 5300 A CAI AC3,DO ; COMPLEMENT AC3( FORM MASK)
895 115E 9469 A LD AC1,@AVPREC ; GET CURRENT VEHICLE PRESENT STATUS
896 115F 3D83 A RAND AC3,AC1 ; MASK OFF PRESENT BIT IN AC1
897 1160          ; DECIDE TO SET, OR LEAVE RESET,THE VEHICLE PRESENT BIT
898 1160 906A A LD ACO,@APRSNT ; GET DATA SENT FROM VCLAS
899 1161 1102 A ROC CCEZ,.,+3 ; IF=0 GO TO VEHICLE NOT PRESENT
900 1162          ; PRESENT, HERE
901 1162 8279 A LD ACO,DBIT(AC2) ; INDEX THRU DBIT TABLE
902 1163 3182 A RXOR ACO,AC1 ; ADD PRESENT BIT BACK IN AC1
903 1164 8469 A ST AC1,@AVPREC ; SAVE NEW VEHICLE PRESENT STATUS
904 1165 2114 A JMP DMORE2 ; SEE IF BUS BIT NEEDS RESETTING
905 1166          ;
906 1166          ;
907 1166          ; VEHICLE WAS CLASSIFIED BY VCLAS
908 1166          ; ( EOS; END OF SIGNATURE WAS FOUND )
909 1166          ;
910 1166          ;

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911 1166          CLASSID:
912 1166 B08A A   ST      ACO,@ACCLASS      ; TEMPORARY SAVE OF TYPE CLASSIFICATION
913 1167          ; ( MADE BY VCLAS )
914 1167 986C A   LD      AC2,@ADCTR        ; FIND CURRENT DETECTOR
915 1168 8279 A   LD      ACO,DBIT(AC2)      ; INDEX THRU DBIT TABLE
916 1169 3381 A   RCPY    ACO,AC3           ; COPY ACO TO AC3
917 116A 5300 A   CAI     AC3,D0           ; COMPLEMENT AC3(FORM MASK)
918 116B 9468 A   LD      AC1,@ABUSWD       ; GET EXISTING 'BUS WORD'
919 116C 3D83 A   RAND    AC3,AC1          ; MASK OFF BUS PRESENT BIT IN AC1
920 116D          ; DECIDE TO SET, OR LEAVE ALONE, THE BUS PRESENT BIT IN AC1
921 116D 908A A   LD      ACO,@ACCLASS      ; RECALL TYPE CLASSIFICATION BY VCLAS
922 116E 1508 A   ROC     CCNZ,CLASS1       ; IF=1 BRANCH TO RESET VEHICLE PRESENT BIT
923 116F          ; ACO=1 FOR NON-BUS
924 116F          ; ACO=0 FOR BUS
925 116F          ; PRESENT, HERE
926 116F 8279 A   LD      ACO,DBIT(AC2)      ; INDEX THRU DBIT TABLE
927 1170 3182 A   RXOR    ACO,AC1          ; ADD BUS PRESENT BIT BACK IN TO AC1
928 1171 B468 A   ST      AC1,@APUSWD       ; SAVE NEW BUS PRESENT WORD
929 1172          ;
930 1172          ; SET COUNTER FOR DCTR TO =1, SINCE BUS WAS JUST DETECTED
931 1172 906C A   LD      ACO,@ADCTR        ; GET DETECTOR NO.
932 1173 886D A   LD      AC2,ACTR         ; GET BASE ADDRESS TO COUNTER
933 1174 3200 A   RADD    ACO,AC2          ; AC2= INDEX TO COUNTER IN USE
934 1175 4C01 A   LI      ACO,C1           ; RESET COUNTER AFTER DETECTING BUS
935 1176 A200 A   ST      ACO,D0(AC2)       ; SET TO =1 FOR BUS PRESENT ( ONLY 1ST PASS)
936 1177          ; COUNTER SET, NOW CONTINUE
937 1177          ;
938 1177          ; RESET VEHICLE PRESENT BIT AT END OF SIGNATURE (EOS)
939 1177 9469 A   CLASS1: LD      AC1,@AVPREC ; GET EXISTING PRESENCE WORD
940 1178 3D83 A   RAND    AC3,AC1          ; AC3 HAS MASK
941 1179 B469 A   ST      AC1,@AVPREC       ; SAVE NEW VEHICLE PRESENCE WORD
942 117A          ;
943 117A          ; DMORE2:
944 117A          ; COME HERE TO SEE IF BUS BIT NEEDS TO BE RESET YET BEFORE GOING
945 117A          ; TO NEXT DETECTOR
946 117A          ;
947 117A 906C A   LD      ACO,@ADCTR        ; GET DETECTOR NO.
948 117B 886D A   LD      AC2,ACTR         ; GET BASE ADDRESS
949 117C 3200 A   RADD    ACO,AC2          ; INDEX FOR THIS DETECTOR
950 117D 8200 A   LD      ACO,D0(AC2)       ; VALUE OF COUNTER IN USE
951 117E 1110 A   ROC     CCFZ,DMORE4       ; IF =0, NO BUS BIT SET IN OUTPUT WORD
952 117F          ; IF NOT=0 INCREMENT COUNTER AND SEE IF MAX. REACHED
953 117F          ; IF MAX. REACHED, RESET BUS BIT IN OUTPUT WORD
954 117F          ;
955 117F 4801 A   AISZ    ACO,C1           ; ACO=ACO+1
956 1180 A200 A   ST      ACO,D0(AC2)       ; SAVE NEW COUNTER VALUE
957 1181 E06E A   SKG     ACO,BUSSET        ; SKIP IF ACO G.T. NO. OF CYCLES TO
958 1182          ; LEAVE BUS BIT SET.
959 1182 21CF A   JMP     DMORE             ; GET NEXT DETECTOR
960 1183          ; ( LEAVE BUS BIT SET FOR NOW )
961 1183          ;
962 1183          ; RESET BUS BIT NOW, THE REQUIRED DELAY HAS EXPIRED.

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REVISION-F 10/02/73  
PBDU PRODUCTION PRDTDTYPE  
DMDN-CPC, LOOP DETECTOR MDNITOR

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PAGE NUMBER 28

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963 1183      ;
964 1183 986C A      LD      AC2,@ADCTR      ; GET CURRENT DETECTDR
965 1184 8279 A      LD      AC0,DBIT(AC2)    ; INDEX THRU DBIT TABLE
966 1185 3381 A      RCPY    AC0,AC3          ; CDPY AC0 TO AC3
967 1186 5300 A      CAI     AC3,D0           ; COMPLEMENT AC3 ( FDRM MASK)
968 1187 9468 A      LD      AC1,@ABUSWD      ; GET CURRENT BUS WORD
969 1188 3083 A      RAND    AC3,AC1          ; RESET BUS BIT IN AC1
970 1189 B468 A      ST      AC1,@ARUSWD      ; SAVE NEW BUS WORD
971 118A      ;
972 118A      ;      ZERO CDUNTER FDR THIS DETECTOR
973 118A 906C A      LD      AC0,@ADCTR      ; GET DETECTOR ND.
974 118B 886D A      LD      AC2,ACTR        ; GET BASE ADDRESS
975 118C 3200 A      RADD    AC0,AC2          ; INDEX FDR THIS DETECTDR
976 118D 4C00 A      LI      AC0,C0           ; AC0=0
977 118E A200 A      ST      AC0,D0(AC2)      ; ZERD THIS DETECTORS COUNTER
978 118F 21C2 A DMDRE4: JMP    DMDRE          ; GET NEXT DETECTDR
979 1190 11B8 A      *=-,+40                  ; EXPANSION
980 1188      ;

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983 11B8      .LIST   LFR
984 11B8      ;
985 11B8      ;     ... ERROR RECORDING ROUTINE ...
986 11B8      ;     UPON ENTRY, AC1=ERROR DATUM
987 11B8      ;     AC3=BASE ADDR OF ERROR RECORDING BUFFER
988 11B8      ;     ENTRY POINT IMPLIES ERROR TYPE
989 11B8      ;
990 11B8      ;
991 11B8      ERE0:
992 11B8 A702 A      ST      AC1,D2(AC3)      ; STORE ERROR DATUM
993 11B9 8301 A      LD      AC0,D1(AC3)      ; FETCH ERROR COUNTER
994 11BA 4801 A      AISZ    AC0,C1          ; INCREMENT
995 11BB 2100 A      JMP     .+1
996 11BC A301 A      ST      AC0,D1(AC3)
997 11BD 8300 A      LD      AC0,D0(AC3)
998 11BE 0720 A      SETBIT  D0              ; SET ERROR FLAG BIT 0
999 11BF A300 A      ST      AC0,D0(AC3)
1000 11C0 0200 A     RTS      D0              ; RETURN FROM ERE0
1001 11C1      ;
1002 11C1      ERE1:
1003 11C1 A704 A      ST      AC1,D4(AC3)      ; STORE ERROR DATUM
1004 11C2 8303 A      LD      AC0,D3(AC3)      ; FETCH ERROR COUNTER
1005 11C3 4801 A      AISZ    AC0,C1          ; INCREMENT
1006 11C4 2100 A      JMP     .+1
1007 11C5 A303 A      ST      AC0,D3(AC3)
1008 11C6 8300 A      LD      AC0,D0(AC3)
1009 11C7 0721 A      SETBIT  D1              ; SET ERROR FLAG BIT 1
1010 11C8 A300 A      ST      AC0,D0(AC3)
1011 11C9 0200 A     RTS      D0              ; RETURN FROM ERE1
1012 11CA      ;
1013 11CA      ERE2:
1014 11CA A706 A      ST      AC1,D6(AC3)      ; STORE ERROR DATUM
1015 11CB 8305 A      LD      AC0,D5(AC3)      ; FETCH ERROR COUNTER
1016 11CC 4801 A      AISZ    AC0,C1          ; INCREMENT
1017 11CD 2100 A      JMP     .+1
1018 11CE A305 A      ST      AC0,D5(AC3)
1019 11CF 8300 A      LD      AC0,D0(AC3)
1020 11D0 0722 A      SETBIT  D2              ; SET ERROR FLAG BIT 2
1021 11D1 A300 A      ST      AC0,D0(AC3)
1022 11D2 0200 A     RTS      D0              ; RETURN FROM ERE2
1023 11D3      ;
1024 11D3      ERE3:
1025 11D3 A708 A      ST      AC1,D8(AC3)      ; STORE ERROR DATUM
1026 11D4 8307 A      LD      AC0,D7(AC3)      ; FETCH ERROR COUNTER
1027 11D5 4801 A      AISZ    AC0,C1          ; INCREMENT
1028 11D6 2100 A      JMP     .+1
1029 11D7 A307 A      ST      AC0,D7(AC3)
1030 11D8 8300 A      LD      AC0,D0(AC3)
1031 11D9 0723 A      SETBIT  D3              ; SET ERROR FLAG BIT 3
1032 11DA A300 A      ST      AC0,D0(AC3)
1033 11DB 0200 A     RTS      D0              ; RETURN FROM ERE3
1034 11DC      ;

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1035 11DC      ERE4:
1036 11DC A70A A      ST      AC1.D10(AC3)      ; STORE ERROR DATUM
1037 11DD 8309 A      LD      AC0.D9(AC3)      ; FETCH ERROR COUNTER
1038 11DE 4801 A      AISZ    AC0.C1          ; INCREMENT
1039 11DF 2100 A      JMP     *+1
1040 11E0 A309 A      ST      AC0.D9(AC3)
1041 11E1 8300 A      LD      AC0.D0(AC3)
1042 11E2 0724 A      SETBIT  D4              ; SET ERROR FLAG BIT 4
1043 11E3 A300 A      ST      AC0.D0(AC3)
1044 11E4 0200 A      RTS     D0              ; RETURN FROM ERE4
1045 11E5      ;
1046 11E5      ERE5:
1047 11E5 A70C A      ST      AC1.D12(AC3)      ; STORE ERROR DATUM
1048 11E6 830B A      LD      AC0.D11(AC3)      ; FETCH ERROR COUNTER
1049 11E7 4801 A      AISZ    AC0.C1          ; INCREMENT
1050 11E8 2100 A      JMP     *+1
1051 11E9 A30B A      ST      AC0.D11(AC3)
1052 11EA 8300 A      LD      AC0.D0(AC3)
1053 11EB 0725 A      SETBIT  D5              ; SET ERROR FLAG BIT 5
1054 11EC A300 A      ST      AC0.D0(AC3)
1055 11ED 0200 A      RTS     D0              ; RETURN FROM ERE5
1056 11EE      ;
1057 11EE      ERE6:
1058 11EE A70E A      ST      AC1.D14(AC3)      ; STORE ERROR DATUM
1059 11EF 830D A      LD      AC0.D13(AC3)      ; FETCH ERROR COUNTER
1060 11F0 4801 A      AISZ    AC0.C1          ; INCREMENT
1061 11F1 2100 A      JMP     *+1
1062 11F2 A30D A      ST      AC0.D13(AC3)
1063 11F3 8300 A      LD      AC0.D0(AC3)
1064 11F4 0726 A      SETBIT  D6              ; SET ERROR FLAG BIT 6
1065 11F5 A300 A      ST      AC0.D0(AC3)
1066 11F6 0200 A      RTS     D0              ; RETURN FROM ERE6
1067 11F7      ;
1068 11F7      ERE7:
1069 11F7 A710 A      ST      AC1.D16(AC3)      ; STORE ERROR DATUM
1070 11F8 830F A      LD      AC0.D15(AC3)      ; FETCH ERROR COUNTER
1071 11F9 4801 A      AISZ    AC0.C1          ; INCREMENT
1072 11FA 2100 A      JMP     *+1
1073 11FB A30F A      ST      AC0.D15(AC3)
1074 11FC 8300 A      LD      AC0.D0(AC3)
1075 11FD 0727 A      SETBIT  D7              ; SET ERROR FLAG BIT 7
1076 11FE A300 A      ST      AC0.D0(AC3)
1077 11FF 0200 A      RTS     D0              ; RETURN FROM ERE7
1078 1200      ;
1079 1200      ;
1080 1200      ;

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1083 1200          .LIST   LVC
1084 1200          VCLAS:
1085 1200          ;      08-29-77
1086 1200          ;      *** VEHICLE CLASSIFIER ***
1087 1200          ;      RETURNS ARE DO WITH AC0=1 FOR NON-BUS, AC0=0 FOR BUS
1088 1200          ;      OR D1 FOR ERROR CONDITION, NO VEHICLE DETECTED
1089 1200          ;      IF VEHICLE IS PRESENT ON SPECIFIED DETECTOR(WORD 8),
1090 1200          ;      PRSNT=1, OTHERWISE PRSNT=0( FOR TESTING BY DMON).
1091 1200          ;      TYPICAL VCLAS DATA BASE
1092 1200          ;
1093 1200          ;      FOR 40 FT AMG MOVING VEHICLE
1094 1200          ;      WORD-0 TOTAL TIME      -03DB HEX
1095 1200          ;      1 FIRST PEAK AMP.    -0081
1096 1200          ;      2 TIME              -00CF
1097 1200          ;      WORD-3 2ND PEAK AMP.    -00A6
1098 1200          ;      -4 TIME              -024D
1099 1200          ;      -5 LAST PEAK AMP.    -008B
1100 1200          ;      6 TIME              -0377
1101 1200          ;      WORD -7 VEHICLE PRESENT- 0100, END OF SIGNATURE -0001
1102 1200          ;
1103 1200          ;
1104 1200          ;
1105 1200 2100 A      JMP      .+1          ; JSR @ACOTF MAY BE INSERTED HERE
1106 1201 9C6C A      LD       AC3,@ADCTR    ; DETECTOR INDEX COUNTER
1107 1202          ;                      IS THE SPECIFIED DETECTOR IN RANGE
1108 1202 ED6E A      SKG      AC3,VCHD      ; MAX. DETS
1109 1203 ED6E A      SKG      AC3,VCLD      ; MIN. INDEX VALUE
1110 1204 215C A      JMP      VCER1        ; NEGATIVE NOT ALLOWED
1111 1205          ;                      LOCATE THIS DETECTOR'S PORTION OF SDB
1112 1205 4BFF A      AISZ     AC3,CM1
1113 1206 2100 A      JMP      .+1
1114 1207 5F03 A      SHL      AC3,D3
1115 1208 8870 A      LD       AC2,AVCSDB
1116 1209 3900 A      RADD     AC2,AC3
1117 120A 8871 A      LD       AC2,AVCDB      ; INDEX TO TEMP. STORAGE FOR SIG. DATA BASE
1118 120B          ;                      CHECK EOS STATUS REGISTER
1119 120B 8307 A      LD       AC0,D7(AC3)    ; CHECK FOR VEHICLE PRESENT BIT IN WORD 8
1120 120C          ;                      OF SPECIFIED DETECTOR
1121 120C 6076 A      AND      AC0,VPRES      ; MASK OFF ALL BUT VEHICLE PRESENT BIT
1122 120D 1103 A      BOC      CCEZ,VNOT      ; BRANCH IF =0 TO LOG NOT PRESENT FOR
1123 120E          ;                      USE BY DMON ROUTINE
1124 120E          ;                      OTHERWISE LOG VEHICLE PRESENT
1125 120E 4C01 A      LI       AC0,C1          ; PRESENT FLAG
1126 120F B06A A      ST       AC0,@APRSNT    ; SAVE VEHICLE PRESENT
1127 1210 2102 A      JMP      .+3          ; GO TO CHECK FOR END OF SIGNATURE
1128 1211 4C00 A      VNOT:    LI       AC0,C0    ; NOT PRESENT FLAG
1129 1212 B06A A      ST       AC0,@APRSNT    ; SAVE VEHICLE NOT PRESENT
1130 1213          ;      CONTINUE, CHECK FOR END OF SIGNATURE
1131 1213 8307 A      LD       AC0,D7(AC3)    ; GET WORD 8 OF SPECIFIED DETECTOR
1132 1214 6075 A      AND      AC0,EOSBIT     ; MASK OFF ALL BUT END OF SIGNATURE
1133 1215 1118 A      BOC      CCEZ,VCRET     ; BRANCH IF NO END OF SIGNATURE BIT SET
1134 1216          ;

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1135 1216      ;
1136 1216      ;
1137 1216      ;
1138 1216      ;
1139 1216 8305 A      LD      AC0,D5(AC3)
1140 1217 A205 A      ST      AC0,D5(AC2)
1141 1218 8300 A      LD      AC0,D0(AC3)
1142 1219 A200 A      ST      AC0,D0(AC2)
1143 121A 8301 A      LD      AC0,D1(AC3)
1144 121B A201 A      ST      AC0,D1(AC2)
1145 121C 8302 A      LD      AC0,D2(AC3)
1146 121D A202 A      ST      AC0,D2(AC2)
1147 121E 8303 A      LD      AC0,D3(AC3)
1148 121F A203 A      ST      AC0,D3(AC2)
1149 1220 8304 A      LD      AC0,D4(AC3)
1150 1221 A204 A      ST      AC0,D4(AC2)
1151 1222 8306 A      LD      AC0,D6(AC3)
1152 1223 A206 A      ST      AC0,D6(AC2)
1153 1224      ;
1154 1224 8307 A      LD      AC0,D7(AC3)
1155 1225      ;
1156 1225 4D00 A      LI      AC1,C0
1157 1226 A707 A      ST      AC1,D7(AC3)
1158 1227 1507 A      BOC     CCNZ,VC01
1159 1228 946C A      LD      AC1,@ADCTR      ; DETECTOR INDEX VALUE
1160 1229 8C72 A      LD      AC3,APERR
1161 122A 2C92 A      JSR     @AERE6
1162 122B 8205 A      LD      AC0,D5(AC2)
1163 122C 1502 A      BOC     CCNZ,VC01
1164 122D 2C93 A      JSR     @AERE7
1165 122E      ;
1166 122E 0201 A VCRET: RTS      D1      ; RETURN FROM VCLAS, NO SIGNATURES IN AC0
1167 122F      ;
1168 122F      ;
1169 122F 4C20 A VC01: LI      AC0,C32      ; TEST FOR NOISE
1170 1230 E200 A      SKG     AC0,D0(AC2)      ; C32=32
1171 1231 210A A      JMP     VC02
1172 1232      ;
1173 1232      ;
1174 1232 946C A      LD      AC1,@ADCTR
1175 1233 8C72 A      LD      AC3,APERR
1176 1234 2C91 A      JSR     @AERE5
1177 1235 4C01 A      LI      AC0,C1
1178 1236 8C73 A      LD      AC3,AVCLOG
1179 1237 7B01 A      ISZ     D1(AC3)
1180 1238 21F5 A      JMP     VCRET      ; RETURN FROM VCLAS, ERROR
1181 1239 7300 A      ISZ     D0(AC3)
1182 123A 3081 A      NOP
1183 123B 21F2 A      JMP     VCRET      ; RETURN FROM VCLAS, ERROR
1184 123C      ;      INCREMENT DETECTOR COUNTER
1185 123C      VC02:
1186 123C 4FFF A      LI      AC3,CM1

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1187	123D	946C	A	LD	AC1,@ADCTR	; DETECTOR INDEX VALUE
1188	123E	3700	A	RADD	AC1,AC3	
1189	123F	CC74	A	ADD	AC3,AVCVC	
1190	1240	7800	A	ISZ	D0(AC3)	
1191	1241	2100	A	JMP	.*+1	
1192	1242					GROSS TEST
1193	1242	4C00	A	LI	AC0,C0	
1194	1243	F205	A	SKNE	AC0,D5(AC2)	
1195	1244	2115	A	JMP	VCGTF	
1196	1245					CHECK MAGNITUDE OF SIGNATURE DATA
1197	1245	812D	A	LD	AC0,VCMA	
1198	1246	7201	A	SKAZ	AC0,D1(AC2)	
1199	1247	211D	A	JMP	VCER2	
1200	1248	7203	A	SKAZ	AC0,D3(AC2)	
1201	1249	211B	A	JMP	VCER2	
1202	124A	7205	A	SKAZ	AC0,D5(AC2)	
1203	124B	2119	A	JMP	VCER2	
1204	124C	8127	A	LD	AC0,VCMT	
1205	124D	7200	A	SKAZ	AC0,D0(AC2)	
1206	124E	211A	A	JMP	VCER3	
1207	124F	7202	A	SKAZ	AC0,D2(AC2)	
1208	1250	2118	A	JMP	VCER3	
1209	1251	7204	A	SKAZ	AC0,D4(AC2)	
1210	1252	2116	A	JMP	VCER3	
1211	1253	7206	A	SKAZ	AC0,D6(AC2)	
1212	1254	2114	A	JMP	VCER3	
1213	1255					CHECK FOR TIME OVERFLOW
1214	1255	811F	A	LD	AC0,VCMOF	
1215	1256	6200	A	AND	AC0,D0(AC2)	
1216	1257	F11D	A	SKNE	AC0,VCMOF	
1217	1258	2152	A	JMP	VCHFE	
1218	1259	2127	A	JMP	VCDHK	
1219	125A	4C01	A	LI	AC0,C1	
1220	125B	8C73	A	LD	AC3,AVCLOG	
1221	125C	7803	A	ISZ	D3(AC3)	
1222	125D	21D0	A	JMP	VCRET	; RETURN FROM VCLAS, ERROR
1223	125E	7802	A	ISZ	D2(AC3)	
1224	125F	2100	A	JMP	.*+1	
1225	1260	21CD	A	JMP	VCRET	; RETURN FROM VCLAS, ERROR
1226	1261			VCER1:		
1227	1261					DETECTOR SPECIFIED DOES NOT EXIST
1228	1261	946C	A	LD	AC1,@ADCTR	; DETECTOR INDEX VALUE
1229	1262	8C72	A	LD	AC3,APERP	
1230	1263	2C8D	A	JSR	@AERE1	
1231	1264	21C9	A	JMP	VCRET	; RETURN FROM VCLAS, ERROR
1232	1265			VCER2:		
1233	1265					VEHICLE SIGNATURE DATA EXCEEDS BOUNDS (AMP)
1234	1265	946C	A	LD	AC1,@ADCTR	
1235	1266	8C72	A	LD	AC3,APERR	
1236	1267	2C8E	A	JSR	@AERE2	
1237	1268	21C5	A	JMP	VCRET	
1238	1269			VCER3:		

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1239 1269	;			VEHICLE SIGNATURE DATA EXCEEDS BOUNOS (TIME)
1240 1269 946C A		LD	AC1,@ADCTR	; DETECTOR INOEX VALUE
1241 126A 8C72 A		LD	AC3,APERR	
1242 126B 2C8F A		JSR	@AERE3	
1243 126C 21C1 A		JMP	VCRET	
1244 126D	VCER4:			
1245 126D	;			VEHICLE TIME DATA OUT OF ORDER
1246 126D 8C72 A		LO	AC3,APERR	
1247 126E 946C A		LD	AC1,@ADCTR	; DETECTOR INDEX VALUE
1248 126F 2C90 A		JSR	@AERE4	
1249 1270 21BD A		JMP	VCRET	

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1252 1271		•LIST	LVC	
1253 1271	;			DETECTOR INDEX RANGE
1254 1271 0010 A	VCHD:	•WORD	DETS	; HIGHEST DETECTOR INDEX NUMBER EXPECTED
1255 1272 0000 A	VCLD:	•WORD	0	; LOWEST DETECTOR INDEX NUMBER - 1
1256 1273	;			MASKS
1257 1273 FF00 A	VCMA:	•WORD	X'FF00	; MASK USED IN AMPLITUDE IN RANGE TEST
1258 1274 F000 A	VCMT:	•WORD	X'F000	; MASK USED IN TIME IN RANGE TEST
1259 1275 0FFF A	VCMOF:	•WORD	X'0FFF	; MASK USED IN TIME OVERFLOW TEST
1260 1276	;			THE FOLLOWING ARE USEO IN VCDHK
1261 1276 0028 A	VCST1:	•WORD	40	; 2.50 B4 USED IN L2 TEST
1262 1277 0007 A	VCST2:	•WORD	7	; 0.43 B4 USED IN L1 TEST
1263 1278 000B A	VCST3:	•WORD	11	; 0.70 B4 USED IN L1 TEST
1264 1279	;			THE FOLLOWING ARE USED IN VCHFE
1265 1279 2BAE A	VC31:	•WORD	11182	; 2.730 B13 G1 COEFFICIENT FOR H1
1266 127A 0E04 A	VC32:	•WORD	3588	; 0.876 B13 G2 COEFFICIENT FOR H1
1267 127B 2851 A	VC41:	•WORD	10321	; 2.520 B13 G1 COEFFICIENT FOR H2
1268 127C 0239 A	VC42:	•WORD	569	; 0.139 B13 G2 COEFFICIENT FOR H2
1269 127D 3EE1 A	H1T1:	•WORD	16097	; 3.93 B13 H1 TEST LOWER BOUND
1270 127E 6785 A	H1T2:	•WORD	26501	; 6.47 B13 H1 TEST UPPER BOUND
1271 127F 3000 A	H2T1:	•WORD	12288	; 3.00 B13 H2 TEST LOWER BOUNO
1272 1280 5000 A	H2T2:	•WORD	20480	; 5.00 B13 H2 TEST UPPER BOUNO

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1275	1281		.LIST	LVC	
1276	1281	VCDHK:			
1277	1281	;			VEHICLE CLASSIFICATION MOVING/STOPPED TEST
1278	1281	;			
1279	1281	;			INSURE TIME DATA WORDS IN PROPER ORDER
1280	1281	8204 A	LD	AC0.D4(AC2)	
1281	1282	E202 A	SKG	AC0.D2(AC2)	
1282	1283	21E9 A	JMP	VCER4	
1283	1284	8206 A	LD	AC0.D6(AC2)	
1284	1285	E204 A	SKG	AC0.D4(AC2)	
1285	1286	21E6 A	JMP	VCER4	
1286	1287	8200 A	LD	AC0.D0(AC2)	
1287	1288	E206 A	SKG	AC0.D6(AC2)	
1288	1289	21E3 A	JMP	VCER4	
1289	128A	;			FORM T(C1) + T(C4) - T(C3)
1290	128A	8200 A	LD	AC0.D0(AC2)	; AC0 = T(C4)
1291	128B	D206 A	SUB	AC0.D6(AC2)	; AC0 = T(C4) - T(C3)
1292	128C	C202 A	ADD	AC0.D2(AC2)	; AC0 = T(C4) - T(C3) + T(C1)
1293	128D	A207 A	ST	AC0.D7(AC2)	; R0
1294	128E	;			FORM F0
1295	128E	8602 A	LD	AC1.D2(AC2)	; R0
1296	128F	5D04 A	SHL	AC1.D4	; B4
1297	1290	4C00 A	LI	AC0.C0	
1298	1291	C172 A	ADD	AC0.VCC0	; CLEAR OVERFLOW STATUS BIT
1299	1292	0690 A	DIV	D7(AC2)	; R4
	1293	0007 A			
1300	1294	2100 A	JMP	.+1	
1301	1295	;			CHECK FOR OVERFLOW. IF OVERFLOW OCCURS
1302	1295	;			JUMP TO VCHFE
1303	1295	074E A	SKSTF	D14	
1304	1296	2101 A	JMP	.+2	
1305	1297	2113 A	JMP	VCHFE	
1306	1298	;			AC1 = T(C1) / T(C1) + T(C4) - T(C3)
1307	1298	;			VEHICLE IS CONSIDERED MOVING VEHICLE IF
1308	1298	;			0.43 < F0 < 0.7
1309	1298	E5DE A	SKG	AC1.VCST2	; SKIP IF AC1 > 0.43
1310	1299	2111 A	JMP	VCHFE	
1311	129A	E5DD A	SKG	AC1.VCST3	; SKIP IF AC1 > 0.7
1312	129B	F5DC A	SKNE	AC1.VCST3	; SKIP IF AC1 NOT = 0.7
1313	129C	210E A	JMP	VCHFE	; JUMP TO STOPPED VEHICLE CLASSIFIER
1314	129D	;			FORM F1 + F2
1315	129D	8606 A	LD	AC1.D6(AC2)	; R0
1316	129E	D602 A	SUB	AC1.D2(AC2)	; AC1 = T(C3) - T(C1)
1317	129F	5D04 A	SHL	AC1.D4	; B4
1318	12A0	4C00 A	LI	AC0.C0	
1319	12A1	C162 A	ADD	AC0.VCC0	; CLEAR OVERFLOW STATUS BIT
1320	12A2	0690 A	DIV	D7(AC2)	; R4
	12A3	0007 A			
1321	12A4	2100 A	JMP	.+1	
1322	12A5	;			CHECK FOR OVERFLOW. IF OVERFLOW OCCURS
1323	12A5	;			JUMP TO VCHFE
1324	12A5	074E A	SKSTF	D14	

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1325	12A6	2101 A	JMP	.+2	
1326	12A7	2103 A	JMP	VCHFE	
1327	12A8	;			AC1 = T(C3) - T(C1) / T(C1) + T(C4) - T(C3)
1328	12A8	;			VEHICLE IS CONSIDERED STOPPED VEHICLE IF
1329	12A8	;			F1 + F2 > 2.5
1330	12A8	E5CD A	SKG	AC1.VCST1	; SKIP IF AC1 > 2.5
1331	12A9	2132 A	JMP	VCKFE	; JUMP TO MOVING VEHICLE CLASSIFIER
1332	12AA	2100 A	JMP	VCHFE	



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1335 12AB		.LIST	LVC	
1336 12AB	;			VEHICLE CLASSIFICATION
1337 12AB	;			STOPPED VEHICLE CLASSIFIER
1338 12AB	VCHFE:			
1339 12AB 8C73 A		LD	AC3,AVCLOG	
1340 12AC 7B05 A		ISZ	D5(AC3)	
1341 12AD 2102 A		JMP	.*+3	
1342 12AE 7B04 A		ISZ	D4(AC3)	
1343 12AF 2100 A		JMP	.*+1	
1344 12B0	;			INCREMENT STOPPED VEHICLE COUNTER
1345 12B0	;			FORM C31 * A1
1346 12B0 85C8 A		LD	AC1,VC31	; B13
1347 12B1 0680 A		MPY	D3(AC2)	
12B2 0003 A				
1348 12B3 A208 A		ST	AC0,D8(AC2)	
1349 12B4 A609 A		ST	AC1,D9(AC2)	
1350 12E5	;			FORM C32 * A2
1351 12B5 85C4 A		LD	AC1,VC32	; B13
1352 12B6 0680 A		MPY	D5(AC2)	
12B7 0005 A				
1353 12B8	;			FORM (C31*A1 + C32*A2) / A0
1354 12B8 06A0 A		DADD	D8(AC2)	; B13
12B9 0008 A				
1355 12BA C149 A		ADD	AC0,VCC0	; CLEAR OVERFLOW STATUS BIT
1356 12BB 0690 A		DIV	D1(AC2)	; B13
12BC 0001 A				
1357 12BD 2100 A		JMP	.*+1	
1358 12BE	;			CHECK FOR OVERFLOW. IF OVERFLOW OCCURS
1359 12BE	;			JUMP TO VCNB5
1360 12BE 074E A		SKSTF	D14	
1361 12BF 2101 A		JMP	.*+2	
1362 12C0 2552 A		JMP	@AVCVNB	IF VEHICLE IS NOT A BUS, JUMP TO VCVNB.
1363 12C1	;			; SKIP IF AC1 > 3.93
1364 12C1 E5BB A		SKG	AC1,H1T1	
1365 12C2 2550 A		JMP	@AVCVNB	
1366 12C3 E5BA A		SKG	AC1,H1T2	; SKIP IF AC1 => 6.47
1367 12C4 2101 A		JMP	.*+2	
1368 12C5 254D A		JMP	@AVCVNB	
1369 12C6	;			FORM C41 * A1
1370 12C6 85B4 A		LD	AC1,VC41	; B13
1371 12C7 0680 A		MPY	D3(AC2)	
12C8 0003 A				
1372 12C9 A208 A		ST	AC0,D8(AC2)	
1373 12CA A609 A		ST	AC1,D9(AC2)	
1374 12CB	;			FORM C42 * A2
1375 12CB 85B0 A		LD	AC1,VC42	; B13
1376 12CC 0680 A		MPY	D5(AC2)	
12CD 0005 A				
1377 12CE	;			FORM (C41*A1 + C42*A2) / A0
1379 12CE 06A0 A		DADD	D8(AC2)	; B13
12CF 0008 A				
1379 12D0 C133 A		ADD	AC0,VCC0	; CLEAR OVERFLOW STATUS BIT

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1380 12D1 0690 A		DIV	D1(AC2)	; B13
12D2 0001 A				
1381 12D3 2100 A		JMP	.*+1	
1382 12D4	;			CHECK FOR OVERFLOW. IF OVERFLOW OCCURS
1383 12D4	;			JUMP TO VCNB5
1384 12D4 074E A		SKSTF	D14	
1385 12D5 2101 A		JMP	.*+2	
1386 12D6 253C A		JMP	@AVCVNB	IF VEHICLE IS NOT A BUS, JUMP TO VCVNB
1387 12D7	;			; SKIP IF AC1 > 3.0
1388 12D7 E5A7 A		SKG	AC1,H2T1	
1389 12D8 253A A		JMP	@AVCVNB	
1390 12D9 E5A6 A		SKG	AC1,H2T2	; SKIP IF AC1 > 5.0
1391 12DA 2537 A		JMP	@AVCBUS	
1392 12DB 2537 A	VCHFE:	JMP	@AVCVNB	

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1395 12DC		•LIST	LVC	
1396 12DC	;			
1397 12DC	;			
1398 12DC	;			
1399 12DC	VCKFE:			
1400 12DC 8C73 A		LD	AC3,AVCLOG	
1401 12DD 7B07 A		ISZ	D7(AC3)	
1402 12DE 2102 A		JMP	•+3	
1403 12DF 7B06 A		ISZ	D6(AC3)	
1404 12E0 2100 A		JMP	•+1	
1405 12E1 8D21 A		LD	AC3,VCCP	
1406 12E2 4C00 A		LI	AC0,C0	
1407 12E3 A20C A		ST	AC0,D12(AC2)	
1408 12E4 A20F A		ST	AC0,D15(AC2)	
1409 12E5	VCK:			
1410 12E5	;			
1411 12E5 8704 A		LD	AC1,D4(AC3)	FORM C4*A2 = G2'
1412 12E6 0680 A		MPY	D5(AC2)	; B13
1413 12F8 A208 A		ST	AC0,D8(AC2)	
1414 12E9 A609 A		ST	AC1,D9(AC2)	
1415 12EA	;			FORM C3*A1 = G1'
1416 12EA 8703 A		LD	AC1,D3(AC3)	; B13
1417 12EB 0680 A		MPY	D3(AC2)	
1418 12ED A20A A		ST	AC0,D10(AC2)	
1419 12EE A60B A		ST	AC1,D11(AC2)	
1420 12EF	;			FORM ABS(G1' - G2') / A0
1421 12FF F208 A		SKNE	AC0,D8(AC2)	; SKIP IF UPPER G1' NOT = UPPER G2'
1422 12F0 2103 A		JMP	•+4	
1423 12F1 E208 A		SKG	AC0,D8(AC2)	; SKIP IF UPPER G1' > UPPER G2'
1424 12F2 212F A		JMP	VCK3	
1425 12F3 2122 A		JMP	VCK21	
1426 12F4 651C A		AND	AC1,VCM15	
1427 12F5 F51B A		SKNE	AC1,VCM15	; SKIP IF BIT 15 IS NOT SET
1428 12F6 2108 A		JMP	VCK1	
1429 12F7 8519 A		LD	AC1,VCM15	
1430 12F8 6609 A		AND	AC1,D9(AC2)	
1431 12F9 F517 A		SKNE	AC1,VCM15	; SKIP IF BIT 15 IS NOT SET
1432 12FA 2127 A		JMP	VCK3	
1433 12FB 860B A	VCK0:	LD	AC1,D11(AC2)	
1434 12FC E609 A		SKG	AC1,D9(AC2)	; SKIP IF LOWER G1' > LOWER G2'
1435 12FD 2124 A		JMP	VCK3	
1436 12FE 2116 A		JMP	VCK2	
1437 12FF 6609 A	VCK1:	AND	AC1,D9(AC2)	
1438 1300 F510 A		SKNE	AC1,VCM15	
1439 1301 21F9 A		JMP	VCK0	
1440 1302 2112 A		JMP	VCK2	

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1443 1303          .LIST    LVC
1444 1303 1304 A VCCP: .WORD VCC0
1445 1304          ;
1446 1304          ;
1447 1304 0000 A VCCO: .WORD 0
1448 1305          ;
1449 1305 046E A      .WORD 1134
1450 1306 0051 A      .WORD 81
1451 1307 03A5 A      .WORD 933
1452 1308 0F26 A      .WORD 3878
1453 1309 0000 A      .WORD 0
1454 130A 1028 A      .WORD 4136
1455 130B          ;
1456 130B 1A8F A      .WORD 6799
1457 130C 15C2 A      .WORD 5570
1458 130D 2298 A      .WORD 8888
1459 130E 4199 A      .WORD 16793
1460 130F 0000 A      .WORD 0
1461 1310 1F1A A      .WORD 7962
1462 1311          ;
1463 1311 8000 A VCM15: .WORD X*8000
1464 1312 1385 A AVCBUS: .WORD VCBUS
1465 1313 138C A AVCVNB: .WORD VCVNB
1466 1314 1381 A AVCER: .WORD VCER

```

THE FOLLOWING IS USED TO CLEAR THE OVERFLOW  
STATUS BIT BEFORE EACH DIVIDE OPERATION

THE FOLLOWING ARE USED IN VCKFE

```

; 0.277 B13    F1 COEFFICIENT FOR K4
; 0.0198 B13   F2 COEFFICIENT FOR K4
; 0.228 B13    G1 COEFFICIENT FOR K4
; 0.947 B13    G2 COEFFICIENT FOR K4

; 1.01 B13     K4 BIAS

; 1.66 B13     F1 COEFFICIENT FOR K5
; 1.36 B13     F2 COEFFICIENT FOR K5
; 2.17 B13     G1 COEFFICIENT FOR K5
; 4.10 B13     G2 COEFFICIENT FOR K5

; 1.944 B13    K5 BIAS

```

MASK

```

; MASK FOR DOUBLE PRECISION COMPARISONS
; POINTER TO VEHICLE IS BUS ROUTINE
; POINTER TO VEHICLE NOT BUS ROUTINE
; POINTER TO OVERFLOW ERROR ROUTINE

```

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1469 1315	.LIST	LVC	
1470 1315			
1471 1315 860B A	VCK2:	LD	AC1,011(AC2)
1472 1316 06B0 A	VCK21:	OSUB	D8(AC2)
1317 0008 A			
1473 1318 C1EB A	ADO	ACO,VCC0	
1474 1319 0690 A	OIV	O1(AC2)	
131A 0001 A			
1475 131B			
1476 131B			
1477 131B 074E A	SKSTF	O14	
1478 131C 2101 A	JMP	.+2	
1479 1310 25F6 A	JMP	@AVCER	
1480 131E A60D A	ST	AC1,013(AC2)	
1481 131F 4C00 A	LI	ACO,C0	
1482 1320 A20C A	ST	ACO,D12(AC2)	
1483 1321 210F A	JMP	VCK5	
1484 1322			
1485 1322 8208 A	VCK3:	LD	ACO,D8(AC2)
1486 1323 8609 A		LD	AC1,D9(AC2)
1487 1324 06B0 A		OSUB	O10(AC2)
1325 000A A			
1488 1326 C1D0 A	ADO	ACO,VCC0	
1489 1327 0690 A	OIV	D1(AC2)	
1328 0001 A			
1490 1329			
1491 1329			
1492 1329 074E A	SKSTF	O14	
1493 132A 2101 A	JMP	.+2	
1494 132B 25E8 A	JMP	@AVCER	
1495 132C			
1496 132C 5101 A	CAI	AC1,C1	
1497 132D A60D A	ST	AC1,013(AC2)	
1498 132E 4C00 A	LI	ACO,C0	
1499 132F 5000 A	CAI	ACO,C0	
1500 1330 A20C A	ST	ACO,012(AC2)	
1501 1331			
1502 1331 8604 A	VCK5:	LD	AC1,D4(AC2)
1503 1332 0602 A		SUB	AC1,D2(AC2)
1504 1333 0780 A		MPY	O1(AC3)
1334 0001 A			
1505 1335 A208 A	ST	ACO,D8(AC2)	
1506 1336 A609 A	ST	AC1,09(AC2)	
1507 1337			
1508 1337 8606 A	LD	AC1,D6(AC2)	
1509 1338 D604 A	SUB	AC1,D4(AC2)	
1510 1339 0780 A	MPY	O2(AC3)	
133A 0002 A			
1511 133B A20A A	ST	ACO,010(AC2)	
1512 133C A60B A	ST	AC1,D11(AC2)	
1513 1330			
1514 1330 F208 A	SKNE	ACO,D8(AC2)	

G1' > G2'

; B13 FORM G1' - G2'

; CLEAR OVERFLOW STATUS BIT

; FORM (G1' - G2') / A0

CHECK FOR OVERFLOW. IF OVERFLOW OCCURS  
JUMP TO VCER

G1' < G2'

; B13

; FORM (G2' - G1') / A0

; CLEAR OVERFLOW STATUS BIT

; FORM (G2' - G1') / A0

CHECK FOR OVERFLOW. IF OVERFLOW OCCURS  
JUMP TO VCER

CONVERT QUOTIENT TO NEGATIVE AND STORE

FORM C11\*(T(C2) - T(C1))

; B0

; B13

FORM C12 \* (T(C3) - T(C2)) = F2'

FORM ABS(F2' - F1')

; SKIP IF UPPER F2' NOT = UPPER F1'

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1515 133E 2103 A      JMP      *.+4
1516 133F E208 A      SKG      ACO*D8(AC2)          ; SKIP IF UPPER F2' > UPPER F1'
1517 1340 2125 A      JMP      VCK9
1518 1341 210E A      JMP      VCK8
1519 1342 65CE A      AND      AC1,VC*15
1520 1343 F5CD A      SKNE     AC1,VC*15          ; SKIP IF BIT 15 NOT SET
1521 1344 2108 A      JMP      VCK7
1522 1345 85CB A      LD       AC1,VC*15
1523 1346 6609 A      AND      AC1,D9(AC2)
1524 1347 F5C9 A      SKNE     AC1,VC*15          ; SKIP IF BIT 15 NOT SET
1525 1348 211D A      JMP      VCK9
1526 1349 860B A      VCK6:    LD       AC1,D11(AC2)
1527 134A E609 A      SKG      AC1,D9(AC2)          ; SKIP IF LOWER F2' > LOWER F1'
1528 134B 211A A      JMP      VCK9
1529 134C 2103 A      JMP      VCK8
1530 134D 6609 A      VCK7:    AND      AC1,D9(AC2)
1531 134E F5C2 A      SKNE     AC1,VC*15
1532 134F 21F9 A      JMP      VCK6
1533 1350          ;
1534 1350 4D00 A      VCK8:    LI       AC1,C0
1535 1351 F60C A      SKNE     AC1,D12(AC2)          ; SKIP IF G2' - G1' NEGATIVE
1536 1352 2139 A      JMP      VCVNB              ; OTHERWISE JUMP TO NON-BUS ROUTINE
1537 1353 820A A      LD       ACO,D10(AC2)          ; B13
1538 1354 860B A      LD       AC1,D11(AC2)
1539 1355 0680 A      DSUB     D8(AC2)
1540 1356 0008 A
1540 1357 C1AC A      ADD      ACO,VCCO          ; CLEAR OVERFLOW STATUS BIT
1541 1358 0690 A      DIV      D7(AC2)
1542 1359 0007 A
1542 135A          ;
1543 135A          ;
1544 135A 074E A      SKSTF    D14
1545 135B 2101 A      JMP      *.+2
1546 135C 25B7 A      JMP      #AVCER
1547 135D 4C00 A      LI       ACO,C0
1548 135E 06A0 A      DADD     D12(AC2)
1549 135F 000C A
1549 1360 3081 A      NOP
1550 1361 07A0 A      DADD     D5(AC3)
1551 1362 0005 A
1551 1363 2100 A      JMP      *.+1
1552 1364 1227 A      BOC      CC2P,VCVNB          ; IF RESULTS =>0, JUMP TO NON-BUS ROUTINE
1553 1365 2114 A      JMP      VCNK
1554 1366          ;
1555 1366 8208 A      VCK9:    LD       ACO*D8(AC2)
1556 1367 8609 A      LD       AC1,D9(AC2)
1557 1368 0680 A      DSUB     D10(AC2)
1558 1369 000A A
1558 136A C199 A      ADD      ACO,VCCO          ; CLEAR OVERFLOW STATUS BIT
1559 136B 0690 A      DIV      D7(AC2)
1560 136C 0007 A
1560 136D          ;

```

CHECK FOR OVERFLOW. IF OVERFLOW OCCURS

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1561 136D      ;                                JUMP TO VCER
1562 136D 074E A      SKSTF  D14
1563 136E 2101 A      JMP     .+2
1564 136F 25A4 A      JMP     @AVCER
1565 1370 A610 A      ST      AC1,D16(AC2)
1566 1371 4C00 A      LI      AC0,C0
1567 1372 8706 A      LD      AC1,D6(AC3)
1568 1373 06B0 A      DSUB    D15(AC2)
1569 1374 000F A
1569 1375 3081 A      NOP
1570 1376 06A0 A      DADD    D12(AC2)
1570 1377 000C A
1571 1378 2100 A      JMP     .+1
1572 1379 1212 A      BOC     CCZP,VCVNB      ; IF RESULTS =>0, JUMP TO NON-BUS ROUTINE
1573 137A      VCNK:
1574 137A FD88 A      SKNE    AC3,VCCP      ; B0
1575 137B 2101 A      JMP     .+2
1576 137C 2108 A      JMP     VCBUS
1577 137D 4C06 A      LI      AC0,C6
1578 137E 3300 A      RADD    AC0,AC3
1579 137F 2500 A      JMP     @AVCK
1580 1380 12E5 A      AVCK: .WORD  VCK
1581 1381      VCER:
1582 1381      ;                                ERROR DETECTED  OVERFLOW ON DIVIDE
1583 1381 946C A      LD      AC1,@ADCTR      ; DETECTOR INDEX VALUE
1584 1382 8C72 A      LD      AC3,APERR
1585 1383 2C8C A      JSR     @AEREO
1586 1384 0201 A      RTS      D1      ; ERROR RETURN FROM VCLASS,
1587 1385      ; NO SIGNATURE PRESENT

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VEHICLE CLASSIFIER-CLASSIFY AS BUS OR NONBUS

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1590 1385      .LIST  LVC
1591 1385      ; *****
1592 1385      ;
1593 1385      ; VEHICLE IS BUS
1594 1385      ;
1595 1385      VCBUS:
1596 1385 4C00 A      LI      AC0,C0      ; SET FOR BUS PRESENT
1597 1386 8C73 A      LD      AC3,AVCLOG
1598 1387 7809 A      ISZ     D9(AC3)
1599 1388 0200 A      RTS      D0      ; AC0=0 F OR BUS DETECTED,
1600 1389      ; RETURN FROM VCLAS
1601 1389 7808 A      ISZ     DR(AC3)
1602 138A 2100 A      JMP     .+1
1603 138B 0200 A      RTS      D0      ; AC0=0 FOR BUS DETECTED,
1604 138C      ; RETURN FROM VCLAS
1605 138C      ;
1606 138C      ;
1607 138C      ;
1608 138C      ; *****
1609 138C      ;
1610 138C      ; VEHICLE IS NON-BUS
1611 138C      ;
1612 138C 4C01 A      VCVNB: LI      AC0,C1
1613 138D 8C73 A      LD      AC3,AVCLOG
1614 138E 730B A      ISZ     D11(AC3)
1615 138F 0200 A      RTS      D0      ; AC0=1 FOR NON-BUS DETECTED,
1616 1390      ; RETURN FROM VCLAS
1617 1390 780A A      ISZ     D10(AC3)
1618 1391 2100 A      JMP     .+1
1619 1392 0200 A      RTS      D0      ; AC0=1 FOR NON-BUS DETECTED,
1620 1393      ; RETURN FROM VCLAS

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1623 1393      ;      .LIST  LER
1624 1393      ;
1625 1393      ;      ... BACKGROUND PROGRAMS ...
1626 1393      ;      2-1-77
1627 1393      ;
1628 1393      ;
1629 1393      EBKD:
1630 1393      ;
1631 1393      ;      ... RAM ADDRESS TEST ...
1632 1393 8096 A EBKD1: LD      AC0,AERAM      ; START ADDRESS ( PAST DEND + DEBUG AREA )
1633 1394 80A8 A      ST      AC0,@ASSAD
1634 1395 80F3 A      LD      AC0,H32FF      ; END  ADDRESS
1635 1396 80A9 A      ST      AC0,@ASEAD
1636 1397      ;
1637 1397 2C2A A      JSR      @ASMAD
1638 1398 2104 A      JMP      EBKDE          ; ERROR RETURN, (AC2) = CONTENTS
1639 1399      ;                          ; (AC3) = ADDRESS
1640 1399 2100 A      JMP      .+1          ; NO ERROR RETURN
1641 139A      ;
1642 139A 0744 A      SKSTF   D4          ; SKIP IF STATUS IS SET
1643 139B 21F7 A      JMP      EBKD1        ; PESTART RAM ADDRESS TEST
1644 139C 2100 A      JMP      EBKDE        ; JUMP IF ERROR
1645 139D      ;
1646 139D      ;      ... ERROR, TERMINAL WAIT LOOP ...
1647 139D      EBKDE:
1648 139D 0B80 A      PFLG     MERR        ; LIGHT MEMORY ERROR INDICATOR
1649 139E      ;                          ; FLAG 11, FAULT-1 LITE
1650 139E 2C27 A      JSR      @AEADC       ; ERROR,  AUTORESTART *****

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1653 139F      ;      .LIST  LER
1654 139F      ;
1655 139F      ;      ... RAM ADDRESS TEST ...
1656 139F      ;
1657 139F 4CFF A SMAD:  LI      AC0,CM1      ; CLEAR ERROR COUNTER
1658 13A0 88A9 A      LD      AC2,ASEAD     ; POINTER TO END ADDRESS
1659 13A1 9CA8 A      LD      AC3,@ASSAD    ; START ADDRESS
1660 13A2      ;
1661 13A2 AF00 A SMAD1: ST      AC3,(AC3)    ; STORE ADDRESS AT EACH LOCATION
1662 13A3 4301 A      AISZ     AC3,C1      ; INCREMENT ADDRESS
1663 13A4 EE00 A      SKG      AC3,(AC2)    ; SKIP IF DONE
1664 13A5 21FC A      JMP      SMAD1
1665 13A6      ;
1666 13A6 9CA8 A      LD      AC3,@ASSAD    ; START ADDRESS
1667 13A7 FF00 A SMAD2: SKNE     AC3,(AC3)    ; SKIP IF MISMATCH
1668 13A8 2107 A      JMP      SMAD3        ; MATCH, CONTENTS = ADDRESS
1669 13A9 4801 A      AISZ     AC0,C1      ; SKIP IF FIRST ERROR
1670 13AA 1301 A      BOC      CCR0,SMAD2    ; BRANCH IF SECOND ERROR
1671 13AB 21FB A      JMP      SMAD2        ; CONTINUE LOOP
1672 13AC      ;
1673 13AC      ;      ... TWO CONSECUTIVE ADDRESS ERRORS ...
1674 13AC 8B00 A SMADE: LD      AC2,(AC3)    ; GET ERRONEOUS CONTENTS
1675 13AD 0704 A      SETST   D4          ; SET STATUS FLAG 4
1676 13AE 0B80 A      PFLG     MERR        ; LIGHT MEMORY ERROR INDICATOR
1677 13AF 2C27 A      JSR      @AEADC       ; ERROR,  AUTORESTART *****
1678 13B0      ;
1679 13B0 4CFF A SMAD3: LI      AC0,CM1      ; CLEAR ERROR COUNTER
1680 13B1 4B01 A      AISZ     AC3,C1      ; INCREMENT ADDRESS
1681 13B2 EE00 A      SKG      AC3,(AC2)    ; SKIP IF DONE
1682 13B3 21F3 A      JMP      SMAD2        ; CONTINUE LOOP
1683 13B4 0201 A      RTS      D1          ; RETURN FROM SMAD (NO ERROR)

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1686 13B5      .LIST   LDR
1687 13B5      .ASECT
1688 13B5 3000 A      .=X'3000
1689 3000      ; *****
1690 3000      ;
1691 3000      ;           ... DATA BASE ...
1692 3000      ;
1693 3000      ;
1694 3000      ;           ... BUS DETECTOR SIGNATURE DATA ...
1695 3000      ;           ( STORED IN VCSDB )
1696 3000      ;           1-25-77
1697 3000      ;           ( UP TO 16 DETECTORS @ 8 WORDS PER SIGNATURE)
1698 3000      ;
1699 3000      ;
1700 3000      ;           WORD 0 - TOTAL SIGNATURE DURATION
1701 3000      ;           1 - AMPLITUDE OF FIRST PEAK
1702 3000      ;           2 - TIME OF FIRST PEAK
1703 3000      ;           3 - AMPLITUDE OF SECOND PEAK
1704 3000      ;           4 - TIME OF SECOND PEAK
1705 3000      ;           5 - AMPLITUDE OF THIRD OR LAST PEAK
1706 3000      ;           6 - TIME OF LAST PEAK
1707 3000      ;           7 - END OF SIGNATURE STATUS, BIT 0 SET
1708 3000      ;           VEHICLE PRESENT STATUS, BIT 8 SET.
1709 3000      ;
1710 3000      ; VCSDB:
1711 3000 3080 A      .=.+128
1712 3080      ;
1713 3080      ;
1714 3080 3081 A BUSWD: .=.+1
1715 3081 3082 A VPREC: .=.+1
1716 3082      ;
1717 3082      ;           ... DATA OUTPUT CPC DATA BASE ...
1718 3082      ;           ; BUS PRESENT WORD
1719 3082 3093 A CTR:  .=.+17
1720 3093      ;           ; VEHICLE PRESENT WORD
1721 3093      ;           ; BIT POSITIONS ARE 16,15,...,3,2,1
1722 3093      ;           ; AND REPRESENT THE CORRESPONDING
1723 3093      ;           ; DETECTOR
1724 3093      ;           ; COUNTERS SHOWING LENGTHENING OF BUS BIT
1725 3093 3094 A DCTR: .=.+1
1726 3094      ;           ; IN OUTPUT WORD
1727 3094 30A4 A VCV:  .=.+16
1728 30A4 30B8 A VCD:  .=.+20
1729 30B8 30B9 A VPRSNT: .=.+1
1730 30B9      ;           ... VEHICLE CLASSIFIER DATA ...
1731 30B9 30BA A CLASS: .=.+1
1732 30BA      ;           ; COUNTER FOR SEQUENCING THRU SIGNATURE DATA
1733 30BA      ;           ; VEHICLE COUNTERS, ONE PER DETECTOR
1734 30BA      ;           ; VEHICLE PRESENT=1 (NOT PRESENT =0)
1735 30BA      ;           ; FOR EACH DETECTOR.
1736 30BA      ;           ; TEMPORARY SAVE LOC. FOR SAVE OF CLASSIFICATION
1737 30BA      ;           ; BY DMON
1738 30BA      ;           ... VEHICLE CLASSIFIER VEHICLE LOG ...
1739 30BA 30BC A      .=.+2
1740 30BC 30BE A      .=.+2
1741 30BE 30C0 A      .=.+2
1742 30C0      ;           ; NUMBER OF SIGNATURES REJECTED AS NOISE
1743 30C0 30C2 A      .=.+2
1744 30C2      ;           ; NUMBER OF GROSS TEST FAILURES
1745 30C2 30C4 A      .=.+2
1746 30C4      ;           ; NUMBER OF VEHICLES HANDLED BY
1747 30C4 30C6 A      .=.+2
1748 30C6      ;           ; STOPPED VEHICLE CLASSIFIER
1749 30C6      ;           ; NUMBER OF VEHICLES HANDLED BY
1750 30C6      ;           ; MOVING VEHICLE CLASSIFIER
1751 30C6      ;           ; NUMBER OF VEHICLES CLASSIFIED
1752 30C6 30C7 A EBUF: .=.+1
1753 30C7      ;           ; AS BUSES
1754 30C7      ;           ; NUMBER OF VEHICLES CLASSIFIED
1755 30C7      ;           ; AS NON-BUSES
1756 30C7      ;           ... EXECUTIVE CPC DATA BASE ...
1757 30C7      ;           ; RTC COMPUTE FLAG

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1738 30BA      ; VCLG:
1739 30BA 30BC A      .=.+2
1740 30BC 30BE A      .=.+2
1741 30BE 30C0 A      .=.+2
1742 30C0      ;
1743 30C0 30C2 A      .=.+2
1744 30C2      ;
1745 30C2 30C4 A      .=.+2
1746 30C4      ;
1747 30C4 30C6 A      .=.+2
1748 30C6      ;
1749 30C6      ;
1750 30C6      ;
1751 30C6      ;
1752 30C6 30C7 A EBUF: .=.+1
1753 30C7      ;
1754 30C7      ;

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DATA BASE - REGISTER SAVE AREAS

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1757 30C7          .LIST   LDR
1758 30C7          ;
1759 30C7          ;
1760 30C7          ;... SAVE AREA FOR RTC INTERRUPTS ...
1761 30C7 30C8 A   ESAVE:  .=.+1          ; AC0
1762 30C8 30C9 A   .=.+1          ; AC1
1763 30C9 30CA A   ESV2:   .=.+1          ; AC2
1764 30CA 30CB A   .=.+1          ; AC3
1765 30CB 30CC A   ESVF:   .=.+1          ; RALU FLAGS
1766 30CC 30DC A   .=.+16         ; STACK SAVE AREA
1767 30DC 30DD A   ESVS:   .=.+1          ; SELECT FLAG STATE
1768 30DD          ;
1769 30DD          ;
1770 30DD          ;... SNAPSHOT (COTF) SAVE AREA ...
1771 30DD 30DE A   CSAV:   .=.+1          ; AC0
1772 30DE 30DF A   .=.+1          ; AC1
1773 30DF 30E0 A   CSV2:   .=.+1          ; AC2
1774 30E0 30E1 A   .=.+1          ; AC3
1775 30E1 30E2 A   CSVF:   .=.+1          ; RALU FLAGS
1776 30E2 30F2 A   .=.+16         ; STACK SAVE AREA
1777 30F2 30F3 A   CSVS:   .=.+1          ; SELECT FLAG STATE
1778 30F3          ;
1779 30F3          ;
1780 30F3          ;... STACKFULL SAVE AREA ...
1781 30F3 30F4 A   ISV0:   .=.+1
1782 30F4 30F5 A   ISV1:   .=.+1
1783 30F5 30F6 A   ISV2:   .=.+1
1784 30F6 30F7 A   ISV3:   .=.+1
1785 30F7 30F8 A   ISTK1:  .=.+1
1786 30F8 30F9 A   ISTK2:  .=.+1
1787 30F9 30FA A   ISTK3:  .=.+1
1788 30FA 30FB A   ISTK4:  .=.+1
1789 30FB 3107 A   ISTK5:  .=.+12
1790 3107          ;
1791 3107          ;
1792 3107          ;
1793 3107          ;... AUTORESTART SAVE AREA ...
1794 3107 3108 A   EDSAV:   .=.+1          ; AC0
1795 3108 3109 A   .=.+1          ; AC1
1796 3109 310A A   EDSV2:  .=.+1          ; AC2
1797 310A 310B A   .=.+1          ; AC3
1798 310B 310C A   EDSVF:  .=.+1          ; RALU FLAGS
1799 310C 311C A   .=.+16         ; STACK SAVE AREA
1800 311C 311D A   EDSVS:  .=.+1          ; SELECT FLAG STATE
1801 311D          ;
1802 311D          ;
1803 311D 3125 A   CTST:   .=.+8          ;... OPTIONAL USE SAVE AREA ...
                                           ; OPTIONAL USE SAVE AREA

```

REVISION-F 10/02/73  
PBDU PRODUCTION PROTOTYPE  
DATA BASE - SELF TEST DATA

08/30/77 9.187  
PAGE NUMBER 51

```

1806 3125          .LIST   LDR
1807 3125          ;
1808 3125          ;
1809 3125 3126 A   SSAD:   .=.+1          ;... SELF TEST DATA BASE ...
                                           ; RAM ADDRESS TEST START ADDRESS
1810 3126 3127 A   SEAD:   .=.+1          ; RAM ADDRESS TEST END ADDRESS
1811 3127 3145 A   .=.+30         ; (EXPANSIBILITY)
1812 3145          ;

```

REVISION-F 10/02/73  
PBDU PRODUCTION PROTOTYPE  
DATA BASE - ERROR DATA

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PAGE NUMBER 52

```

1815 3145          .LIST  LDB
1816 3145          ;
1817 3145          ;
1818 3145          ;
1819 3145          ;
1820 3145          ;
1821 3145          ;
1822 3145          ;
1823 3145 3146 A PERR:  .=.+1          ; ERROR BUFFER FLAG (SET CONDITION, BIT = 1)
1824 3146          ; BIT 0, ARITHMETIC OVERFLOW
1825 3146          ; BIT 1, OUT OF RANGE (VCLASS DETECTOR INDEX)
1826 3146          ; BIT 2, DATA EXCEEDS BOUNDS (VEHICLE AMP)
1827 3146          ; BIT 3, DATA EXCEEDS BOUNDS (VEHICLE TIME)
1828 3146          ; BIT 4, DATA SEQUENCE ERROR (VEHICLE TIME)
1829 3146          ; BIT 5, DATA VALIDITY ERROR (NOISE)
1830 3146          ; BIT 6, EOS STATUS WORD ALTERED DURING COPY
1831 3146          ; OPERATION
1832 3146          ; BIT 7, SIGNATURE LOST DURING COPY OPERATION
1833 3146          ; BIT 8, OUT OF RANGE (PREQ DETECTOR INDEX)
1834 3146          ; THE FOLLOWING, BIT 8,9, ARE NOT USED
1835 3146          ; BIT 9, DATA VALIDITY ERROR ( ATTEMPT
1836 3146          ; TO PREEMPT DOWNSTREAM VEHICLE)
1837 3146          ; BIT 9, NON-POSITIVE DURATION OF SOURCE
1838 3146          ; EXCHANGE INTERVAL AT PREEMPT MOD
1839 3146          ;
1840 3146 315A A      .=.+20          ; (ERROR COUNTER, ERROR WORD)
1841 315A          ;
1842 315A          ;
1843 315A          ;
1844 315A          ;
1845 315A 315B A EERR:  .=.+1          ; ERROR FLAGS (SET CONDITION, BIT = 1)
1846 315B          ; BIT 0, RTC ERROR
1847 315B          ; BIT 1, DCR1.NE.DOCW1
1848 315B          ; BIT 2, DCR2.NE.DOCW2
1849 315B          ; BIT 3, MORE THAN ONE RESET HIGH
1850 315B          ; BIT 4, DETECTOR UNDERCOUNTING
1851 315B          ; (TOTAL FOR ALL DETECTORS,
1852 315B          ; INDEX OF LAST DETECTOR)
1853 315B          ; BIT 5, INVALID DET INDEX
1854 315B 315D A EERRO:  .=.+2          ; ERROR COUNTER, ERROR WORD
1855 315D 315F A EERR1:  .=.+2          ; ERROR COUNTER, ERROR WORD
1856 315F 3161 A EERR2:  .=.+2          ; ERROR COUNTER, ERROR WORD
1857 3161 3163 A EERR3:  .=.+2          ; ERROR COUNTER, ERROR WORD
1858 3163 3165 A EERR4:  .=.+2          ; ERROR COUNTER, ERROR WORD
1859 3165 3167 A EERR5:  .=.+2          ; ERROR COUNTER, ERROR WORD
1860 3167          ;
1861 3167          ;
1862 3167          ;
1863 3167          ;
1864 3167 3187 A EDERR:  .=.+32          ; (ERROR COUNTER, ERROR DATUM)
1865 3187          ; FOR 16 DETECTORS
1866 3187          ;

```

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PBDU PRODUCTION PROTOTYPE  
DATA BASE - ERROR DATA

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```

1867 3187          ;
1868 3187 3188 A DEND:  .=.+1          ; LAST LOCATION IN READ/WRITE DATA BASE
1869 3188          ; 2-9-77

```

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PBOU PRODUCTION PROTOTYPE  
TOP PAGE PROM-( FF00-FFFF )

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```

1872 3188      .LIST      1
1873 3188      .ASECT
1874 3188 FF00 A      .X'FF00
1875 FF00      ; LOCATIONS X'FF00 THRU X'FFF6 SHALL BE FILLED WITH X'FFFF PRIOR TO
1876 FF00      ;      BURNING PROM
1877 FF00      ;      ( A SKIP INSTRUCTION )
1878 FF00 FFF7 A      .X'F7
1879 FFF7 2D01 A      JSR      @.+2      ; AUTO RESTART ( SHOULD NEVER GET HERE )
1880 FFF8 2D00 A      JSR      @.+1      ; AUTO RESTART ( SHOULD NEVER GET HERE )
1881 FFF9 100D A      .WORD      EADC
1882 FFFA EFCE A      .WORD      X'EFCE      ; CCU ROM START ADDRESS +X'CE
1883 FFFB 25FE A      JMP      @.-1
1884 FFFC EFD9 A      .WORD      X'EFD9      ; CCU ROM START ADDRESS +X'D9
1885 FFFD 25FE A      JMP      @.-1
1886 FFFE 2000 A      JMP      0      ; RESTART INITIALIZATION
1887 FFFF 21FF A      JMP      .      ; LOOP HERE FOR CCU PSEUDO HALT

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PBDU PRODUCTION PROTOTYPE  
LIST DIRECTIVES

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PAGE NUMBER 55

```

1888 0000      .PAGE      ' LIST DIRECTIVES '
1889 0000      .LIST      1
1890 0000 0001 A LAC      =      1
1891 0000 0001 A LBP      =      1
1892 0000 0001 A LER      =      1
1893 0000 0001 A LVC      =      1
1894 0000 0001 A LEB      =      1
1895 0000 0001 A LOB      =      1
1896 0000 0001 A LBX      =      1
1897 0000 0001 A LDM      =      1
1898 0000      .EXT0

```

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PBDU PRODUCTION PROTOTYPE

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```

1901 0000      .LIST      1
1902 0000      .ENO

```

\*\*\*\*\* 0 ERRORS IN ASSEMBLY \*\*\*\*\*

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PBDU PRODUCTION PROTOTYPE

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PAGE NUMBER 57

ABUSWD	AC0	AC1	AC2	AC3	ACCU	ACCUI	ACDISP	ACCLASS	ACMU
0068 A	0000 A	0001 A	0002 A	0003 A	00E2 A	10BC A	10BE A	008A A	00E1 A
ACOTF	ACRAM	ACSAV	ACSV2	ACSVF	ACSVS	ACTF	ACTR	ACTST	ACWAP
0029 A	10BF A	009B A	009C A	009D A	009E A	0095 A	006D A	00A7 A	10C0 A
ADBIT	ADCTR	ADEND	ADMON	AEADC	AEBKD	AEBUF	AECCU	AECCUR	AECER
006B A	006C A	0094 A	0078 A	0027 A	0024 A	0077 A	0022 A	10C1 A	0025 A
AEDSV2	AEDSVF	AEDSVS	AEERR	AEGIS	AEMAD	AERAM	AEREO	AERE1	AERE2
00A4 A	00A5 A	00A6 A	008B A	0021 A	0023 A	0096 A	008C A	008D A	008E A
AERE3	AERE4	AERE5	AERE6	AERE7	AERSI	AESAV	AESCH	AESV2	AESVF
008F A	0090 A	0091 A	0092 A	0093 A	0020 A	0097 A	0026 A	0098 A	0099 A
AESVS	AISTK1	AISTK2	AISTK3	AISTK4	AISV2	APERR	APRSNT	ARST	ARTC
009A A	00A0 A	00A1 A	00A2 A	00A3 A	009F A	0072 A	006A A	0005 A	00E0 A
ASEAD	ASMAD	ASSAD	AVCBUS	AVCDR	AVCER	AVCK	AVCLAS	AVCLOG	AVCSDB
00A9 A	002A A	00A8 A	1312 A	0071 A	1314 A	1380 A	006F A	0073 A	0070 A
AVCVC	AVCVN8	AVPREC	AXRTC	BUSSET	BUSWD	C0	C1	C125	C15
0074 A	1313 A	0069 A	0028 A	006E A	3080 A	0000 A	0001 A	007D A	000F A
C2	C3	C32	C4	C48	C5	C6	C7	C8	CCAR
0002 A	0003 A	0020 A	0004 A	0030 A	0005 A	0006 A	0007 A	0008 A	000F A
CCB0	CCB1	CCCF	CCCU	CCEZ	CCNZ	CCPH	CCSF	CCZN	CCZP
0003 A	0004 A	000E A	000C A	0001 A	0005 A	000D A	0008 A	000B A	0002 A
CLASFI	CLASS	CLASS1	CM1	CM10	CM100	CM110	CM16	CM2	CM20
1166 A	30B9 A	1177 A	FFFF A	FFF6 A	FF9C A	FF92 A	FFF0 A	FFFE A	FFEC A
CM6	COTF	COTF1	COTF2	COTF3	COTF4	COTF5	CSAV	CSV2	CSVF
FFFA A	1109 A	1114 A	1125 A	1127 A	1138 A	113B A	30DD A	30DF A	30E1 A
CSV5	CTR	CTST	D0	D1	D10	D11	D116	D118	D12
30F2 A	3082 A	311D A	0000 A	0001 A	000A A	000B A	0074 A	0076 A	000C A
D13	D14	D15	D16	D17	D18	D19	D2	D20	D21
000D A	000E A	000F A	0010 A	0011 A	0012 A	0013 A	0002 A	0014 A	0015 A
D22	D23	D24	D25	D26	D3	D4	D5	D6	D7
0016 A	0017 A	0018 A	0019 A	001A A	0003 A	0004 A	0005 A	0006 A	0007 A
D8	D9	DBIT	DCTR	DEND	DETS	DM1	DM12	DM2	DM4
0008 A	0009 A	0079 A	3093 A	3187 A	0010 A	FFFF A	FFF4 A	FFFE A	FFFC A
DM7	DMON	DMORE	DMORE1	DMORE2	DMORE4	EADC	EADC1	EBKD	EBKD1
FFF9 A	1150 A	1152 A	1158 A	117A A	118F A	10DD A	10ED A	1393 A	1393 A



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EBKDE	EBUF	ECCU	ECCU1	ECCUI	ECCUR	ECER	EDERR	EDLAY	EDSAV
139D A	30C6 A	10A4 A	10AD A	10BD A	10RB A	10A1 A	3167 A	10DC A	3107 A
EDSV2	EDSVF	EDSV5	EFRR	EERR0	EFRR1	EERR2	EERR3	EERR4	EERR5
3109 A	310B A	311C A	315A A	315B A	315D A	315F A	3161 A	3163 A	3165 A
FERRF	EGIS	EGIS1	EGIS2	EGIS4	EGIS5	EHLT	EMAD	EMADE	EOSBIT
315A A	1023 A	102F A	1040 A	1089 A	108C A	101C A	10C2 A	10C9 A	0075 A
FRE0	FRE1	ERE2	ERE3	ERE4	ERE5	ERE6	ERE7	ERSI	ERTC
11B8 A	11C1 A	11CA A	11D3 A	11DC A	11E5 A	11EE A	11F7 A	1000 A	106D A
FRTC1	ERTS	ESAV	ESCH	ESTK	ESTK1	ESV2	ESVF	ESVS	EZDB
107A A	10DB A	30C7 A	10CC A	1043 A	105A A	30C9 A	30CB A	30DC A	1017 A
FC0	FC03	FC05	FC07	FC1	H0200	H1T1	H1T2	H2T1	H2T2
0000 A	0003 A	0005 A	0007 A	0001 A	00F2 A	127D A	127E A	127F A	1280 A
H32FF	H3300	H33CF	INEN	ISTK1	ISTK2	ISTK3	ISTK4	ISTK5	ISV
00F3 A	00F0 A	00F1 A	0001 A	30F7 A	30F8 A	30F9 A	30FA A	30FB A	30F3 A
ISV0	ISV1	ISV2	ISV3	LAC	LBP	LBX	LDB	LDM	LEB
30F3 A	30F4 A	30F5 A	30F6 A	0001 A	0001 A	0001 A	0001 A	0001 A	0001 A
LER	LVC	MERR	PERR	PERRF	SEAD	SELF	SMAD	SMAD1	SMAD2
0001 A	0001 A	0003 A	3145 A	3145 A	3126 A	0002 A	139F A	13A2 A	13A7 A
SMAD3	SMADE	SSAD	VC01	VC02	VC31	VC32	VC41	VC42	VCBUS
13R0 A	13AC A	3125 A	122F A	123C A	1279 A	127A A	127B A	127C A	1385 A
VCC0	VCCP	VCD8	VCDHK	VCER	VCER1	VCER2	VCER3	VCER4	VCGETF
1304 A	1303 A	30A4 A	1281 A	1381 A	1261 A	1265 A	1269 A	126D A	125A A
VCHD	VCHE	VCHFE	VCK	VCK0	VCK1	VCK2	VCK21	VCK3	VCK5
1271 A	12DB A	12AB A	12E5 A	12FB A	12FF A	1315 A	1316 A	1322 A	1331 A
VCK6	VCK7	VCK8	VCK9	VCKFE	VCLAS	VCLD	VCL0G	VCN15	VCMA
1349 A	134D A	1350 A	1366 A	12DC A	1200 A	1272 A	30BA A	1311 A	1273 A
VCN0F	VCMT	VCNK	VCRET	VCSD8	VCST1	VCST2	VCST3	VCVC	VCVNB
1275 A	1274 A	137A A	122E A	3000 A	1276 A	1277 A	1278 A	3094 A	138C A
VNOT	VPREC	VPRES	VPRSNT	VTEST	XRTC				
1211 A	3081 A	0076 A	30B8 A	1105 A	10FE A				

CAE8 0722

SNUMB = PBDU , ACTIVITY # = 02 , , REPORT CODE = 74 , RECORD COUNT = 000021

PROU 02 08-30-77 9.222

PAGE 1

ORIGIN DATE MODULE ENTRY LOCATION ENTRY LOCATION ENTRY LOCATION ENTRY LOCATION ENTRY LOCATION

SUBPROGRAMS INCLUDED IN DECK.

\$ OPTIONS FORTRAN,NO\*AR  
\$ LIBRARY L1

SUBPROGRAMS OBTAINED FROM USERS LIBRARY L1

SUBPROGRAMS OBTAINED FROM SYSTEM LIBRARY

	RANGE	SIZE
ALLOCATED CORE	000000 THRU 047777	050000
RELOCATABLE	003050 THRU 047777	044730
\$ RRMFL	L1,R,R,USERLIB/UTILITY/BUTIL	
\$ FILE	10,X1R	
\$ FILE	11,X2R,40L	
\$ FILE	51,X3R,44R	

FCB AND BUFFER SPACE		
AVAILABLE	000101 THRU 003047	002747
FILE CTRL BLKS	002644 THRU 003050	000205
MAXIMUM BUFFER SPACE REQUIRED		002404

20K, IS THE MINIMUM MEMORY NEEDED TO LOAD THIS ACTIVITY WITH ALL FILES OPEN 740808 2/H  
001316 LOCATIONS REQUIRED FOR LOAD TABLE  
EXECUTION PROGRAM ENTERED AT 047356 THROUGH .FSETU

SNUMB = PBDU , ACTIVITY # = 02 , , REPORT CODE = 06 , RECORD COUNT = 000746

191 AFUSWD

37 AC0

739	918	928	968	970					
329	347	348	366	368	379	401	405	407	408
425	426	428	429	431	432	439	440	441	442
443	444	445	446	447	448	449	450	454	459
478	497	501	502	503	505	506	508	511	512
528	529	532	553	554	556	560	584	585	590
594	604	605	607	608	610	631	632	633	634
654	670	671	690	695	700	702	703	739	741
747	766	770	772	773	790	791	793	794	796
797	802	818	823	844	845	847	851	870	873
876	877	878	879	892	893	898	901	902	912
915	916	921	926	927	931	933	934	935	947
949	950	955	956	957	965	966	973	975	976
977	993	994	996	997	999	1004	1005	1007	1008
1010	1015	1016	1018	1019	1021	1026	1027	1029	1030
1032	1037	1038	1040	1041	1043	1048	1049	1051	1052
1054	1059	1060	1062	1063	1065	1070	1071	1073	1074
1076	1119	1121	1125	1126	1128	1129	1131	1132	1139
1140	1141	1142	1143	1144	1145	1146	1147	1148	1149
1150	1151	1152	1154	1162	1169	1170	1177	1193	1194
1197	1198	1200	1202	1204	1205	1207	1209	1211	1214
1215	1216	1219	1280	1281	1283	1284	1286	1287	1290
1291	1292	1293	1297	1298	1318	1319	1348	1355	1372
1379	1406	1407	1408	1413	1418	1421	1423	1473	1481
1482	1485	1488	1498	1499	1500	1505	1511	1514	1516
1537	1540	1547	1555	1558	1566	1577	1578	1596	1612
1632	1633	1634	1635	1657	1669	1679			

38 AC1

402	410	421	455	464	474	479	539	550	561
591	596	691	705	716	767	775	786	830	841
852	895	896	902	903	918	919	927	928	939
940	941	968	969	970	992	1003	1014	1025	1036
1047	1058	1069	1156	1157	1159	1174	1187	1188	1228
1234	1240	1247	1295	1296	1309	1311	1312	1315	1316
1317	1330	1346	1349	1351	1364	1366	1370	1373	1375
1388	1390	1411	1414	1416	1419	1426	1427	1429	1430
1431	1433	1434	1437	1438	1471	1480	1486	1496	1497
1502	1503	1506	1508	1509	1512	1519	1520	1522	1523
1524	1526	1527	1530	1531	1534	1535	1538	1556	1565
1567	1583								

39 AC2

353	355	367	368	369	371	399	400	401	402
403	411	413	415	417	419	420	452	453	454
455	456	463	466	468	470	472	473	477	478
479	480	481	496	497	500	501	502	505	506
508	512	527	529	540	541	542	544	546	548
559	560	561	562	563	592	594	595	599	600
601	602	605	608	669	672	688	689	690	691
692	706	708	710	712	714	715	764	765	766
767	768	776	778	780	782	784	785	831	832
833	835	837	839	850	851	852	853	854	891
892	901	914	915	926	932	933	935	948	949
950	956	964	965	974	975	977	1115	1116	1117
1140	1142	1144	1146	1148	1150	1152	1162	1170	1194
1198	1200	1202	1205	1207	1209	1211	1215	1280	1281
1283	1284	1286	1287	1290	1291	1292	1293	1295	1299

1315	1316	1320	1347	1348	1349	1352	1354	1356	1371
1372	1373	1376	1378	1380	1407	1408	1412	1413	1414
1417	1418	1419	1421	1423	1430	1433	1434	1437	1471
1472	1474	1480	1482	1485	1486	1487	1489	1497	1500
1502	1503	1505	1506	1508	1509	1511	1512	1514	1516
1523	1526	1527	1530	1535	1537	1538	1539	1541	1548
1555	1556	1557	1559	1565	1568	1570	1658	1663	1674
1681									

40	AC3	328	354	359	360	361	380	384	385	403	412
		413	414	415	416	417	418	419	456	458	465
		466	467	468	469	470	471	472	480	515	516
		517	521	522	542	543	544	545	546	547	548
		549	562	653	692	694	707	708	709	710	711
		712	713	714	737	768	777	778	779	780	781
		782	783	784	801	817	833	834	835	836	837
		838	839	840	853	893	894	896	916	917	919
		940	966	967	969	992	993	996	997	999	1003
		1004	1007	1008	1010	1014	1015	1018	1019	1021	1025
		1026	1029	1030	1032	1036	1037	1040	1041	1043	1047
		1048	1051	1052	1054	1058	1059	1062	1063	1065	1069
		1070	1073	1074	1076	1106	1108	1109	1112	1114	1116
		1119	1131	1139	1141	1143	1145	1147	1149	1151	1154
		1157	1160	1175	1178	1179	1181	1186	1188	1189	1190
		1220	1221	1223	1229	1235	1241	1246	1339	1340	1342
		1400	1401	1403	1405	1411	1416	1504	1510	1550	1567
		1574	1578	1584	1597	1598	1601	1613	1614	1617	1659
		1661	1661	1662	1663	1666	1667	1667	1674	1680	1681
302	ACCU	NOT USED									
616	ACCU1	584									
618	ACDISP	611									
239	ACCLASS	912 921									
300	ACMU	737									
178	ACOTF	661 721									
619	ACRAM	607									
270	ACSAV	NOT USED									
271	ACSV2	764 765 850 854									
272	ACSVF	773 776 844									
273	ACSVS	794 797 823 831									
256	ACTF	348 809									
199	ACTR	932 948 974									
285	ACTST	NOT USED									
620	ACWAP	592 599									

195	ADBIT	NOT USED									
197	ADCTR	873	876	878	891	914	931	947	964	973	1106
		1159	1174	1187	1228	1234	1240	1247	1583		
255	ADEND	371									
218	ADMON	663									
176	AEADC	483	569	641	1650	1677					
173	AEBKD	384									
216	AEBUF	496	527								
171	AECCU	336									
621	AECCUR	604									
174	AECER	509									
281	AEDSV2	688	689								
282	AEDSVF	703	706								
283	AEDSVS	NOT USED									
241	AEERR	500									
170	AEGIS	161									
172	AEMAD	340									
259	AERAM	631	1632								
243	AEREO	1585									
244	AERE1	1230									
245	AERE2	1236									
246	AERE3	1242									
247	AERE4	1248									
248	AEPE5	1176									
249	AERE6	1161									
250	AERE7	1164									

169	AERSI							
		158						
265	AESAV							
		NOT USED						
175	AESCH							
		519						
266	AESV2							
		399	400	559	563			
267	AESVF							
		408	411	553				
268	AFSV5							
		429	432	532	540			
276	AISTK1							
		440						
277	AISTK2							
		443						
278	AISTK3							
		446						
279	AISTK4							
		449	463					
275	AISV2							
		452	453	477	481			
208	APERR							
		1160	1175	1229	1235	1241	1246	1584
193	APRSNT							
		898	1126	1129				
149	ARST							
		724						
299	ARTC							
		328	380	458	653	694	801	817
290	ASEAD							
		634	1635	1658				
182	ASMAD							
		636	1637					
289	ASSAD							
		632	1633	1659	1666			
1464	AVCBUS							
		1391						
206	AVCDB							
		1117						
1466	AVCER							
		1479	1494	1546	1564			
1580	AVCK							
		1579						
204	AVCLAS							
		885						
209	AVCLOG							
		1178	1220	1339	1400	1597	1613	
205	AVCSDB							
		367	1115					
210	AVCVC							
		1189						



1465	AVCVNE	1362	1365	1368	1386	1389	1392				
192	AVPREC	741	895	903	939	941					
177	AXRTC	665									
200	BUSSET	957									
1714	BUSWD	191									
109	C0	329	366	428	459	528	590	610	654	695	793
		802	818	976	1128	1156	1193	1297	1318	1406	1481
		1498	1499	1534	1547	1566	1596				
121	C125	NOT USED									
118	C15	NOT USED									
110	C1	355	369	379	425	431	503	511	595	672	790
		796	877	934	955	994	1005	1016	1027	1038	1049
		1060	1071	1125	1177	1219	1496	1612	1662	1669	1680
111	C2	NOT USED									
119	C32	1169									
112	C3	464									
120	C48	591									
113	C4	410	473	539	705	775	830				
114	C5	NOT USED									
115	C6	1577									
116	C7	NOT USED									
117	C8	NOT USED									
139	CCAR	738									
128	CCB0	427	792	1670							
129	CCB1	NOT USED									
138	CCCF	659									
133	CCCU	581									

126	CCEZ											
130	CCNZ	498	533	824	899	951	1122	1133				
		922	1158	1163								
134	CCPH											
		376	718									
131	CCSF											
		326	397									
132	CCZN											
		NOT USED										
127	CCZP											
		1552	1572									
911	CLASFI											
		887										
939	CLASS1											
		922										
1731	CLASS											
		239										
102	CM100											
		NOT USED										
105	CM10											
		NOT USED										
101	CM110											
		NOT USED										
104	CM16											
		353										
108	CM1											
		359	421	474	515	550	596	716	747	786	841	
		1112	1186	1657	1679							
103	CM20											
		NOT USED										
107	CM2											
		NOT USED										
106	CM6											
		608										
777	CCTF1											
		787										
796	COTF2											
		792										
800	COTF3											
		795										
827	COTF4											
		824										
832	COTF5											
		842										
763	COTF											
		178										
1770	CSAV											
		270										
1773	CSV2											
		271										

1775	CSVF	272								
1777	CSV5	273								
1719	CTR	199								
1803	CTST	285								
64	D0	389	497	506	507	508	512	529	548	613
		675	743	750	839	856	870	882	894	917
		950	956	967	977	997	998	999	1000	1008
		1011	1019	1021	1022	1030	1032	1033	1041	1043
		1052	1054	1055	1063	1065	1066	1074	1076	1077
		1142	1170	1181	1190	1205	1215	1286	1290	1599
		1615	1619							1603
74	D10	1036	1418	1487	1511	1537	1557	1617		
91	D116	671								
92	D118	670								
75	D11	1048	1051	1419	1433	1471	1512	1526	1538	1614
76	D12	601	1047	1407	1482	1500	1535	1548	1570	
77	D13	1059	1062	1480	1497					
78	D14	602	1058	1303	1324	1360	1384	1477	1492	1544
79	D15	1070	1073	1408	1568					1562
80	D16	1069	1565							
81	D17	426	791							
82	D18	NOT USED								
83	D19	NOT USED								
65	D1	403	413	456	466	480	502	505	546	562
		708	768	778	837	853	993	996	1009	1143
		1166	1179	1198	1356	1380	1474	1489	1504	1586
84	D20	NOT USED								1683
85	D21	NOT USED								
86	D22	NOT USED								

87	D23	NOT USED									
88	D24	NOT USED									
89	D25	NOT USED									
90	D26	NOT USED									
66	D2	415	468	501	544	710	780	835	992	1020	1145
		1146	1207	1223	1281	1292	1295	1316	1503	1510	
67	D3	417	470	542	605	712	782	833	1004	1007	1031
		1114	1147	1148	1200	1221	1347	1371	1416	1417	
68	D4	339	419	420	472	714	715	784	785	1003	1042
		1149	1150	1209	1280	1284	1296	1317	1342	1411	1502
		1509	1642	1675							
69	D5	342	1015	1018	1053	1139	1140	1162	1194	1202	1340
		1352	1376	1412	1550						
70	D6	343	1014	1064	1151	1152	1211	1283	1287	1291	1315
		1403	1508	1567							
71	D7	344	1026	1029	1075	1119	1131	1154	1157	1293	1299
		1320	1401	1541	1559						
72	D8	1025	1348	1354	1372	1378	1413	1421	1423	1472	1485
		1505	1514	1516	1539	1555	1601				
73	D9	1037	1040	1349	1373	1414	1430	1434	1437	1486	1501
		1523	1527	1530	1556	1598					
219	DBIT	195	879	892	901	915	926	965			
1725	DCTR	197									
1868	DEND	255	256	259							
94	DETS	219	1254								
59	DM12	594									
63	DM1	402	455	479	561	691	767	852			
62	DM2	401	454	478	560	690	766	851			
61	DM4	541	832								
60	DM7	600									

870	DMON	218		
884	DMORE1	881		
943	DMORE2	904		
978	DMORE4	951		
874	DMORE	959	978	
707	EADC1	717		
686	EADC	176	1881	
1632	EPKD1	1643		
1629	ERKD	173		
1647	ERKDE	1638	1644	
1752	ERUF	216		
594	ECCU1	597		
578	ECCU	171		
617	ECCUI	585		
613	ECCUR	582	587	621
568	ECER	174		
1863	EDERR	NOT USED		
677	EDLAY	669		
1793	EDSAV	NOT USED		
1796	EDSV2	281		
1798	EDSVF	282		
1800	EDSV5	283		
1854	EERRO	NOT USED		
1855	EERR1	NOT USED		
1856	EERR2	NOT USED		
1857	EERR3	NOT USED		

1858	EERR4	NOT USED	
1859	EERR5	NOT USED	
1844	EERR	241	
1845	EERRF	NOT USED	
412	EGIS1	422	
431	EGIS2	427	
536	EGIS4	533	
541	EGIS5	551	
396	EGIS	170	
376	EHLT	NOT USED	
627	EMAD	172	
641	EMADE	637	
211	EOSBIT	1132	
991	EREO	243	
1002	ERE1	244	
1013	ERE2	245	
1024	ERE3	246	
1035	ERE4	247	
1046	ERE5	248	
1057	ERE6	249	
1068	ERE7	250	
325	ERSI	169	
511	ERTC1	498	
496	ERTC	430	433
675	ERTS	667	
1760	ESAV	265	



652	ESCH	175			
465	ESTK1	475			
438	ESTK	326	397		
1763	ESV2	266			
1765	ESVF	267			
1767	ESVS	268			
368	EZDB	372			
52	FC03	330	460	696	803
53	FC05	381	819		
54	FC07	331	655	697	804
42	FC0	740	749		
43	FC1	742	748		
313	H0200	347			
1269	H1T1	1364			
1270	H1T2	1366			
1271	H2T1	1388			
1272	H2T2	1390			
314	H32FF	633	1634		
311	H3300	NOT USED			
312	H33CF	NOT USED			
146	INEN	333	461	657	698
1785	ISTK1	276			
1786	ISTK2	277			
1787	ISTK3	278			
1788	ISTK4	279			
1789	ISTK5	NOT USED			

1781	ISV0	NOT USED							
1782	ISV1	NOT USED							
1783	ISV2	275							
1784	ISV3	NOT USED							
1780	ISV	NOT USED							
1890	LAC	32							
1891	LBP	152	165	185	263	294	307		
1896	LBX	732							
1895	LDB								
1897	LDM	1686	1757	1806	1815				
1894	LEB	859							
1892	LER	1623	1653						
1893	LVC	319	393	575	624	649	682	754	983
148	MERR	1083	1252	1275	1335	1395	1443	1469	1590
1822	PERR	1648	1676						
1823	PERRF	208							
1810	SEAD	NOT USED							
147	SELF	290							
1661	SMAD1	534	536	825	827				
1667	SMAD2	1664							
1679	SMAD3	1671	1682						
1657	SMAD	1668							
1674	SMADE	182							
1809	SSAD	1670							
1169	VC01	289							
1185	VC02	1158	1163						
		1171							

1265	VC31									
		1346								
1266	VC32									
		1351								
1267	VC41									
		1370								
1268	VC42									
		1375								
1595	VCBUS									
		1464	1576							
1447	VCC0									
		1298	1319	1355	1379	1444	1473	1488	1540	1558
1444	VCCP									
		1405	1574							
1728	VCD8									
		206								
1276	VCDHK									
		1218								
1226	VCER1									
		1110								
1232	VCER2									
		1199	1201	1203						
1238	VCER3									
		1206	1208	1210	1212					
1244	VCER4									
		1282	1285	1288						
1581	VCER									
		1466								
1219	VCGTF									
		1195								
1254	VCHD									
		1108								
1392	VCHE									
		NOT USED								
1338	VCHFE									
		1217	1305	1310	1313	1326	1332			
1433	VCK0									
		1439								
1437	VCK1									
		1428								
1472	VCK21									
		1425								
1471	VCK2									
		1436	1440							
1485	VCK3									
		1424	1432	1435						
1502	VCK5									
		1483								
1526	VCK6									
		1532								
1530	VCK7									
		1521								

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[illegible]

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# APPENDIX E FIELD TEST DATA

Field test data taken on 9/19/77, 9/26/77, and 10/13/77 are summarized in Tables E-1, E-2, and E-3, respectively.

TABLE E-1. SUMMARY OF 9/19/77 FIELD TEST DATA

Time	Bus No.	Direction	Upstream Classification Time (sec)	Downstream Classification Time (sec)	Phase Termination Time (sec)				Preempts		
					Ø2 - 1	Ø4 - 1	Ø2 - 2	Ø4 - 2	Inter-action	Ø4 Force Off	Ø2 Extension
0814	390	N	7.5	15.5	47	90					
0815	1427	S	10.5	---	47	90					
0832	1603	S	3.5	---	47				*		
0834	642	N	67	79	47	70	137		*	20	
0842	390	S	64	71.5	47	66	137			24	
0851	875	N	39	45	47	90					
0859	642	S	1.5	---	47	90					
0916	861	N	28.5	36.5	47	90					
0921	875	S	11.5	---	47	90					
0925	1485	N	63	71.5	47	66	137			24	
0946	861	S	54	---	47	63	137		*	27	
0947	870	N	155	167	137	158	227		*	22	
1000	1485	S	46.5	---	50	67	137			23	3
1005	881	N	2	10	47	90					
1021	870	S	3.5	8.5	47	90					
1025	886	N	84	104	47	87	137			3	
1041	886	S	42	---	47	63	137			27	
1049	1446	N	69.5	78	47	73	137			17	
1100	881	S	5	---	47						
1107	1440	N	43	51.5	47	90					
1121	1446	S	4	---	47						
1123	865	N	11	14	47						
1140	865	S	22	27	47						
1147	367	N	18	0	47						
1201	1440	S	69.5	86	47	79	137			11	
1208	1441	N	34.5	92	47	90					

\* Same cycle or sequential.

TABLE E-1. SUMMARY OF 9/19/77 FIELD TEST DATA (CONCLUDED)

Time	Bus No.	Direction	Upstream Classification Time (sec)	Downstream Classification Time (sec)	Phase Termination Time (sec)			Preempts		
					ø2 - 1	ø4 - 1	ø2 - 2 ø4 - 2	Inter-action	ø4 Force Off	ø2 Extension
1224	367	S	15	---	47					
1227	1427	N	17.5	20.5	47					
1240	1427	S	78.5	---	47	81.5	137		8.5	
1245	886	N	62.5	91.5	47	79	137		11	
1300	1441	S	43.5	49	48			ø		1
1301	881	N	66.5	85	48	80		ø	10	
1321	886	S	41.5	---	47	90				
1325	1446	N	76.5	110	47	80	137		10	
1341	1446	S	29	33.5	47	90				
1348	865	N	55	94	47	90				
1400	881	S	48	---	47	90				
1411	1440	N	79	88	47	81.5	137		8.5	
1423	865	S	27.5	33.5	47	90				
1427	367	N	65.5	90.5	47	79.5	137		10.5	
1440	367	S	70.5	---	47	79	137		11	
1444	1427	N	33	38	47	90				
1502	1440	S	71	---	47	79	137	ø	11	
1503	1441	N	137.5	183	137	180		ø		
1522	1427	S	7	---	47	90				
1525	886	N	29.5	48	48	90				1
1547	1441	S	54.5	96.5	47	90	137			
1551	886	N	66.5	83	47	79	140	ø	11	
1552	334	N	125	139.5	140	180		ø		3
1602	886	S	4	---	47	90		ø		
1603	392	N	10	14	47	90		ø		
1605	886	S	26	32	47	90				
Total									289.5	8
Avg.									15.24	2

ø Same cycle or sequential.



TABLE E-2. SUMMARY OF 9/26/77 FIELD TEST DATA

Time	Bus. No.	Direction	Upstream Classification Time (sec.)	Downstream Classification Time (sec.)	Phase Termination Time (sec.)				Inter-action	Preempts	
					Ø 2 - 1	Ø 4 - 1	Ø 2 - 2	Ø 4 - 2		Ø 4 Force Off	Ø 2 Extension
0803	880	S	27.5	---	50	90					
0816	340	N	85	105	50	88	146	180	*	2	
0817	1512	S	130.5	---	146	180			*		6
0832	394	S	82	---	50	86	135	175	*	4	
0833	631	N	171	182.5	135	174.5	225	270	*	4.5	
0843	340	S	3.5	11	50						
0848	534	N	26	31.5	50						
0859	631	S	48.5	---	52.5	70.5	125			19.5	2.5
0908	903	N	0	4.0	50						
0922	534	S	41	---	50	90					
0925	367	N	40	0	50	90					
0947	903	S	0	32.2	50						
0948	535	N	42.2	47	50	90					
1002	367	S	0	0							
1010	562	N	15	21	50						
1023	535	S	45.5	---	50	68	125			22	
1025	365	N	17.5	24.3	50						
1041	365	S	75	---	50	78.5	129			10.5	
1048	648	N	29	35	50	90					
1101	562	S	8.5	---	50						
1108	1422	N	57	73.2	50	68	125			22	
1123	648	S	53.5	---	50	68	125			22	
1127	898	N	51	76.5	50	68	114	180		22	
1144	898	S	21.2	28	50						
1147	1480	N	43	50.5	50.5	90					0.5
1205	1422	S	36	48.5	50	90					

\* Same cycle or sequential.

TABLE E-2. SUMMARY OF 9/26/77 FIELD TEST DATA (CONCLUDED)

Time	Bus. No.	Direction	Upstream Classification Time (sec)	Downstream Classification Time (sec)	Phase Termination Time (sec)				Inter-action	Preempts	
					ø 2 - 1	ø 4 - 1	ø 2 - 2	ø 4 - 2		ø 4 Force Off	ø 2 Extension
1210	880	N	67	86	50	70.5	125			19.5	
1222	1480	S	0	3.8	50						
1229	1512	N	57.5	102	50 *	68	125	180		22	
1241	1512	S	32.5	---	50	90					
1246	365	N	61.6	78	50	68	125	180		22	
1305	880	S	25	---	50	90					
1306	562	N	1.6	16.7	50						
1322	365	S	54	---	50	68	125	180	*	22	
1323	648	N	63.5	82	50	68	125	180	*	22	
1342	898	N	87.5	109.5	50	90	140	180			
1348	648	S	5	---	50	90					
1401	562	S	45	52	50	90					
1407	1422	N	51	73	50	68	125	180		22	
1421	898	S	88.5	---	50	90	140				
1425	1480	N	62.3	71.5	50	68	125	180		22	
1441	1480	S	5	---	50						
1446	1512	N	43	93	50	90	140	180			
1502	1422	S	56.5	---	50	68	125	180		22	
1504	880	N	24.5	44	50	90	140	180			
1524	1512	S	39.5	---	56	90	140				
1532	384	N	18	36.3	50	90					
1551	880	S	36	---	54.5	90			*		4.5
1552	365	N	0	31	53.3	90	140		*		3.3
1553	188	N	42	52.3	53.3	90	140				3.3
1604	365	S	81	---	50	84	135	180		6	
1607	330	N	27.6	43	50	90	140	174	*		
1608	384	S	38	43	50	90	140	174	*		
Total										308	20.1
Avg.										17.1	3.35

\* Same cycle or sequential.

TABLE E-3. SUMMARY OF 10/13/77 FIELD TEST DATA

Time	Bus. No.	Direction	Upstream Classification Time (sec.)	Downstream Classification Time (sec.)	Phase Termination Time (sec.)				Inter-action	Preempts	
					φ2 - 1	φ4 - 1	φ2 - 2	φ4 - 2		φ4 Force Off	φ2 Extension
0807	1449	N	66.0	77.5	36	69.0			*	21.0	
0807	732	N	73.0	80.5	36	69.0			*	21.0	
0813	379	S	52.0	---	36	55.0				35.0	
0825	656	N	64.5	72.5	36	67.0				23.0	
0828	1449	S	6.0	22.5	36						
0835	779	N	62.5	77.5	36	68.5				21.5	
0840	732	S	6.0	13.0	36						
0845	391	N	39.0	57.0	36	52.0				38.0	
0900	779	S	74.5	87.0	36	77.0	136	166.5	*	13.0	
0901	895	N	163.5	181.5					*	13.5	
0923	856	N	29.0	31.5	36				*		
0924	391	S	28.0	---	36				*		
0941	895	S	42.5	---	36	52.0				38.0	
0952	710	N	79.5	93.5	36	83.0				7.0	
1006	856	S	79.0	---	36	82.0			*	8.0	
1006	390	N	115.5	121.5			126		*		
1022	710	S	0	---							
1026	351	N	62.5	82.5	36	65.5				24.5	
1042	357	S	77.5	---	36	81.0				9.0	
1048	1465	N	24.5	93.0	36	90.0					
1101	390	S	68.5	84.5	36	71.5				18.5	
1103	868	N	20.0	92.0	36	90.0					
1121	1465	S	8.5	---	36						
1125	874	N	63.5	0	36	66.5				23.5	
1140	874	S	0	---							
1147	903	N	26.0	94.5	36	90.0					

\*Same cycle or sequential.

TABLE E-3. SUMMARY OF 10/13/77 FIELD TEST DATA (CONCLUDED)

Time	Bus. No.	Direction	Upstream Classification Time (sec.)	Downstream Classification Time (sec.)	Phase Termination Time (sec.)				Inter-action	Preempts	
					ø 2 - 1	ø 4 - 1	ø 2 - 2	ø 4 - 2		ø 4 Force Off	ø 2 Extension
1201	868	S	58.0	69.5	36	61.0				29.0	
1212	873	N	33.0	59.0	38	54.0				36.0	2
1221	903	S	85.0	---	36	88.0				2.0	
1228	379	N	65.5	84.5	36	69.0	126				
1241	379	S	18.0	---	36				*		
1242	351	N	16.0	27.5	36				*		
1258	390	N	8.5	20.5	36				*		
1259	873	S	73.0	80.0		76.0	126		*	14.0	
1320	351	S	15.5	---	36	90.0	126	180.0			
1332	1465	N	78.5	105.0	36	81.5				8.5	
1341	874	N	23.0	28.0	36	90.0					
1344	1465	S	57.5	71.0	36	68.0				22.0	
1359	390	S	50.5	58.5	36	53.5				36.5	
1408	868	N	64.0	92.5	36	68.0				22.0	
1418	874	S	51.5	63.5	36	55.0				35.0	
1423	903	N	46.0	60.5	36	52.0				38.0	
1439	1431	S	22.5	26.5	36						
1446	903	S	2.5	---	36						
1449	379	N	61.0	0	36	64.0				26.0	
1502	868	S	24.0	29.5	36						
1520	379	S	67.5	---	36	71.0			*	19.0	
1521	873	N	100.5	115.5			126		*		
1525	447	N	85.0	109.5	36	88.0				2.0	
1546	351	N	7.0	27.5	36						
1554	873	S	75.5	89.5	36	78.5			*	11.5	
1554	447	S	79.5	93.0	36	78.5			*	11.5	
1557	292	N	56.0	71.0	36	59.5			*	30.5	
1558	351	S	101.5	106.5	36	59.5	126		*	30.5	
1608	738	N	10.0	18.5	36						
Total										709.5	2
Avg.										21.5	2

\* Same cycle or sequential

## FEDERALLY COORDINATED PROGRAM OF HIGHWAY RESEARCH AND DEVELOPMENT (FCP)

The Offices of Research and Development of the Federal Highway Administration are responsible for a broad program of research with resources including its own staff, contract programs, and a Federal-Aid program which is conducted by or through the State highway departments and which also finances the National Cooperative Highway Research Program managed by the Transportation Research Board. The Federally Coordinated Program of Highway Research and Development (FCP) is a carefully selected group of projects aimed at urgent, national problems, which concentrates these resources on these problems to obtain timely solutions. Virtually all of the available funds and staff resources are a part of the FCP, together with as much of the Federal-aid research funds of the States and the NCHRP resources as the States agree to devote to these projects.\*

### 3. Environmental Considerations in Highway Design, Location, Construction, and Operation

Environmental R&D is directed toward identifying and evaluating highway elements which affect the quality of the human environment. The ultimate goals are reduction of adverse highway and traffic impacts, and protection and enhancement of the environment.

### 4. Improved Materials Utilization and Durability

Materials R&D is concerned with expanding the knowledge of materials properties and technology to fully utilize available naturally occurring materials, to develop extender or substitute materials for materials in short supply, and to devise procedures for converting industrial and other wastes into useful highway products.

Activities are all directed toward the goals of lowering the cost of highway construction and extending the period of maintenance-free operation.

### 5. Design to Reduce Costs, Extend Service Life, and Insure Structural Reliability

R&D is concerned with furthering the technological advances in structural deterioration processes, and construction techniques to provide safe, efficient highways at the lowest possible cost.

### 6. Development and Implementation of New Research

Research is concerned with developing and applying research and technology into practice as it has been commonly identified. "Technology transfer."

### 7. Technology for Highway Maintenance

Research R&D objectives include the development and application of new technology to management, to augment the utilization of resources, and to increase operational efficiency in the maintenance of highway

FCP C

### 1. Improved Safety for Safer

Safety Research the results of the Federal Highway Administration and include standard physical of improvement

### 2. Reduce Traffic Improvements

Traffic operation advanced existing the balance such as motorist

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ADMINISTRATION  
REPORT NO. FH

\* The complete report is available for purchase (NTIS), \$45 price \$45 volume and Analysis (Federal Highway Administration)

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